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Research on the expansion and optimization control strategy of cascaded rectifier H-bridge

Jingpeng Hu[1,2*]

*Correspondence:
02092@bitzh.edu.cn

[1] Beijing Institute of Technology, Beijing, China
[2] Beijing Institute of Technology, Zhuhai, Zhuhai, China

Abstract

Extensive research on the multi-bridge extension of cascaded rectifier stages is deemed important to meet the requirements of high-voltage and high-power applications. Two control structures for capacitor voltage balancing in cascaded rectifier stages are analyzed in this paper. On this basis, the balance strategy for the multi-bridge extension of single-phase cascaded rectifiers is explored. The balance method of ultra-fast balance modulation trajectories is introduced into single-phase multi-bridge cascaded rectification, and the optimal control strategy is selected through simulation verification and comparative analysis. During the actual experiments, some disturbance factors were introduced into the system, causing an instantaneous unbalanced state. However, through the control strategy proposed in this paper, the system can quickly regain balance. Through simulation validation and analysis of the experimental results, the reliability and innovation of this control strategy have been demonstrated.

Keywords: Cascaded rectifier stages, H-bridge extension, Optimization control

Introduction

The research on the expansion and optimization control strategy of cascaded rectifier H-bridge is of great significance for improving Energy conversion efficiency, system performance, and sustainable development. By improving power semiconductor devices and control strategies, energy loss can be reduced, system response speed and stability can be improved, multi-functional integration can be achieved, new energy development can be adapted, and smart grid construction can be promoted. Based on a comprehensive analysis of the literature, the current main control part has complex calculations and a heavy burden on the controller. Therefore, this paper will conduct in-depth research on appropriate control structures and strategies to simplify the control structure and select the optimal control strategy.

Methods

This paper will analyze two control structures: centralized control structure for multiple H-bridge cascade expansion and distributed control structure for multiple H-bridge cascade expansion. It will delve into the balanced strategy for single-phase cascade rectifier

H-bridge expansion and introduce the balancing method of ultra-fast balancing modulation trajectory into single-phase multi-bridge cascade rectification. Finally, a simulation based on two-dimensional modulation will be conducted to explore the cascade rectifier H-bridge expansion and optimization control strategies.

Control structure of cascaded rectifier stage capacitor voltage balance control

By designing and optimizing the control structure, effective capacitor voltage balancing can be achieved, avoiding damage to power equipment caused by high or low capacitor voltage, ensuring uniform current distribution, and improving the power factor and efficiency of the system. This helps to improve the operational efficiency of the power system, reduce maintenance costs, and promote the application of clean energy. Different control structures require different balanced control strategies, and there are significant differences in expansion methods.3

A. Centralized control structure of cascade rectifier capacitor voltage balance

The control of the cascade rectifier stage can be roughly divided into three parts: the main control part, the balance part, and the modulation part.

(1) The main control part is the main function of implementing the rectification system. If the rectifier stage system is operated at a unit power factor, the system transfers active energy to the backward stage, or the system is operated in an active inverter state, or the system only provides reactive energy to the power grid;
(2) The balance part is to achieve balanced control of the DC side capacitor voltage of the H-bridge at all levels of the rectifier stage;
(3) The modulation part is the PWM modulation strategy used. Such as the phase-shifting carrier modulation method, specific harmonic elimination modulation method, and space vector modulation method.

The main control strategies mentioned in references [1–3] for cascaded rectification all utilize independent voltage PI feedback loops. The voltage balancing strategy is closely related to the main control section of the rectification system, while the modulation section remains relatively independent. This control approach requires the adoption of N PI controllers (N being the number of cascaded H-bridges) for the voltage loop: one overall PI voltage controller is used to stabilize the sum or average voltage across the DC side capacitors of each bridge, and N-1 independent PI controllers are employed to stabilize the voltages across the DC sides of each cascaded H-bridge. This results in a complex main control section with a relatively heavy computational burden on the controllers. However, the advantage of this design is that the modulation section is comparatively simpler and can be implemented using analog circuits, among other methods.

B. Cascaded rectifier stage with decentralized control structure for capacitor voltage balancing

Correspondingly to the centralized control structure, the balance and modulation parts are combined with the main control part of the rectifier system for decentralized

control. Through modulation strategies, the capacitor voltage balance of the cascaded rectifier stage system at all levels of the H-bridge is achieved, thereby omitting the PI controller that balances the DC side capacitor voltage of each bridge [4, 5]. The control concept of the voltage loop in the rectifier stage system is to stabilize the total voltage on the DC side of each bridge to be equal to Nu_{dc}^{*} (N is the number of cascaded H-bridges, u_{dc}^{*} is the command voltage on the DC side of a single H-bridge). By modulating the capacitor voltage on the DC side of each cascaded H-bridge to be equal, the capacitor voltage on the DC side of each bridge can ultimately be stabilized at

$$\frac{Nu_{dc}^{*}}{N} = u_{dc}^{*} \tag{1}$$

This paper adopts this control structure. The advantage of this control structure is that the balancing and modulation parts are independent of the main control section of the rectifier stage system. The main control section no longer needs to undergo control transformations for different topological structures, which simplifies its computations. It also makes the transfer of control strategies in the main control section simple when expanding the functionalities of the rectifier stage. The drawback is that the modulation part becomes relatively complex. However, by adopting a modular design and setting independent modulation controllers, the computational burden on the main control section can be greatly reduced.

Multi H-bridge cascading expansion of three single-phase cascaded rectifier stages

A. Centralized control structure multiple H-bridge cascade expansion

Firstly, taking references [4, 5] as examples, the extension of the centralized control structure in cascaded rectifier systems with multiple H-bridges is elucidated. According to reference [6], where $u_{con} \approx u_s$ is assumed, the corresponding control block diagram is shown in Fig. 1. Additionally, the control block diagram proposed in reference [1] for chained STATCOM control is depicted in Fig. 2, where ϕ represents the angle between the inductor current (i_s) and the output voltage (u_{con}) of the cascaded H-bridge on the AC-side.

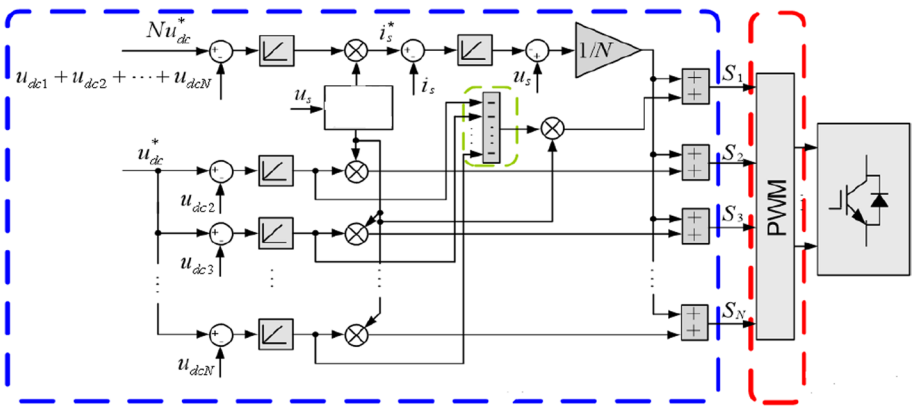


Fig. 1 Rectifier-level multi-H-bridge expansion control diagram

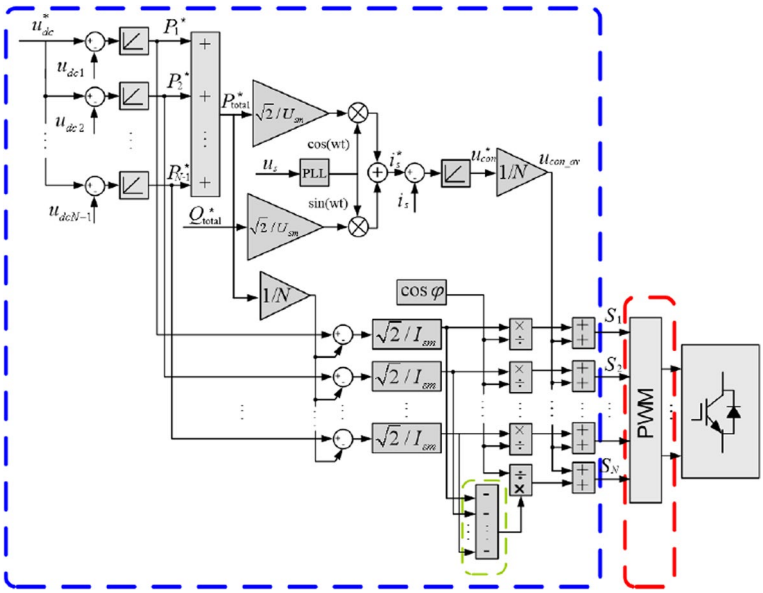


Fig. 2 Chain-type STATCOM multi-H-bridge expansion control

Analyzing Figs. 1 and 2, it can be seen that one is from the perspective of voltage, and the other is from the perspective of power, but both are essentially aimed at redistributing the active energy obtained by each bridge. The average modulation wave u_{con}/N of the output voltage waveform on the AC side of the cascaded H-bridge is obtained through the overall voltage or power loop. Based on this, the modulation waveform required for each bridge is obtained by correcting the difference between the DC side capacitor voltage of each bridge and the command voltage, forming a control loop to ultimately balance the capacitor voltage of each bridge. In order for the cascaded H-bridge to ultimately output the required u_{con}, the centralized control structure must use one H-bridge in the cascade structure as modulation compensation to compensate for the difference after adjustment of other bridges, such as the S_1 bridge in Fig. 1 and the S_N bridge in Fig. 2, which can be called a compensation bridge.

The expansion form of the centralized control structure is relatively simple, similar to the cascade rectification of two bridges. After the load imbalance of each bridge occurs, an independent voltage control loop controller allows each bridge to balance again for a longer time. In practical systems, the H-bridge with sudden load changes is unpredictable, so the saturation upper and lower limits of each independent voltage controller become quite complex. Without setting corresponding saturation controllers, the degree of load imbalance between each bridge cannot be fully expanded.

B. Distributed control structure multiple H-bridge cascade expansion

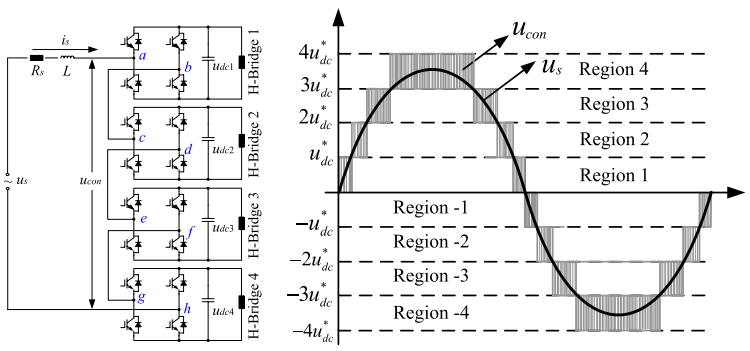
References [6, 7] adopts hysteresis PWM current control method as the main control part of cascade rectification. When expanding, it is still approximately assumed that $u_{con} \approx u_s$. Firstly, the u_{con} to be synthesized is divided into 2N modulation intervals based on the instruction voltage u_{dc}^{*} of a single H-bridge, and the current modulation interval of us is determined. Then, the capacitor voltages on the DC side of the H-bridge at all

levels were sorted. Based on the different absorbed power of the H-bridge under different states, five working states of the H-bridge were defined: "1" state, "0" state, "-1" state, "PWM" state, and "-PWM" state. The "PWM" state is a state that switches between the "1" state and the "0" state based on the output voltage of the H-bridge; The "-PWM" state is a state that switches between the "-1" state and the "0" state based on the output voltage of the H-bridge. References [8, 9] determine the output voltage of the H-bridge in the "PWM" state based on the hysteresis current, and finally uses the step wave stacking method to complete the required modulation part. This modulation method can be abbreviated as the step wave stacking method.

The following is an example of using four H-bridge cascaded rectifiers to illustrate the expansion method of multiple H-bridge cascades in references [4, 5]. The topology structure of the four-bridge cascade rectifier is shown in Fig. 3a. If the capacitor voltage on the DC side of the H-bridge at all levels is equal, the AC side of the four-bridge cascade rectifier can output up to nine levels of step waves. Therefore, u_{con} can be divided into 8 modulation intervals, as shown in Fig. 3b.

According to the magnitude of the DC-side voltages, the four cascaded H-bridges are sorted as follows: $u_{dc1} \le u_{dc2} \le u_{dc3} \le u_{dc4}$. This assumption is used throughout the following analysis. If u_s and i_s have the same phase and $u_s > 0$, the order of functional quantities for the five operating states is as follows: "1" state > "PWM" state " > 0" state " > -PWM" state > " − 1" state. If u_s and i_s have oppose-phase and $u_s > 0$, the order of functional quantities for the five operating states is as follows: "1″ state < "PWM" state < "0″ state " < -PWM" state < "-1″ state. Similarly, the relationship between functional quantities for different bridge states can be derived for the case of $u_s < 0$. Based on this principle, optimization of the modulation section was performed in references [6, 8] to balance the capacitor voltages on the DC side of each bridge, resulting in the working states of each bridge within different modulation intervals as shown in Tables 1 and 2.

Observing Table 1, it can be observed that the modulation schemes of H-bridge 1, H-bridge 2 in Region 1, Region 2, Region -1, and Region -2 generally resemble the modulation scheme based on two-dimensional modulation for fast balancing modulation trajectories. The difference lies in the modulation partitioning. According to references [8, 9], the partitioning is based on the DC-side command voltage udc*.



(a)The topology of CHBR with four cells (b)The output waveform of CHBR with four cells in its AC side

Fig. 3 CHBR with four cells. **a** The topology of CHBR with four cells. **b** The output waveform of CHBR with four cells in its AC side

Table 1 Operation states of H-bridges of CHBR in different regions when u_{con} and i_s have same signs

Partition	*H-bridge 1*	*H-bridge 2*	*H-bridge 3*	*H-bridge 4*
Region 1	PWM	0	0	0
Region 2	1	PWM	0	0
Region 3	1	1	PWM	0
Region 4	1	1	1	PWM
Region -1	-PWM	0	0	0
Region -2	-1	-PWM	0	0
Region -3	-1	-1	-PWM	0
Region -4	-1	-1	-1	-PWM

Table 2 Operation states of H-bridges of CHBR in different regions when u_{con} and i_s have alternative signs

Partition	*H-bridge 1*	*H-bridge 2*	*H-bridge 3*	*H-bridge 4*
Region 1	0	0	0	PWM
Region 2	0	0	PWM	1
Region 3	0	PWM	1	1
Region 4	PWM	1	1	1
Region -1	0	0	0	-PWM
Region -2	0	0	-PWM	-1
Region -3	0	-PWM	-1	-1
Region -4	-PWM	-1	-1	-1

On the other hand, the partitioning in two-dimensional modulation is based on the actual values of the DC-side voltages of each bridge. In the subsequent discussion, we elaborate on the results brought by these two partitioning methods. For now, we approximate that within these four modulation regions, H-bridge 1 and H-bridge 2 adopt fast-balancing modulation trajectories in Region 1, Region 2, Region -1, and Region -2, respectively. Similarly, H-bridge 3 and H-bridge 4 adopt fast-balancing modulation trajectories in Region 3, Region 4, Region -3, and Region -4.

There are three main issues with the modulation strategy in references [7, 8]:

(1) The partitioning of the staircase waveform. Due to the partitioning based on the DC-side capacitor's command voltage u_{dc}^{*} for u_{con} in each individual H-bridge, there can be a phenomenon of modulation failure during periods when the capacitor voltages are unbalanced. In Region 1 as shown in Fig. 3, since $u_{dc1} < u_{dc}^{*}$, H-bridge 1 cannot output the corresponding ucon when $u_{dc1} < u_{con} < u_{dc}^{*}$. At this point, the modulation points of H-bridge 1 and H-bridge 2 in the two-dimensional modulation have exceeded the two-dimensional modulation region. This results in increased fluctuations in the synthesized u_{con} waveform at each step, thereby affecting the quality of the inductor current waveform. The partitioning should be revised to consider the actual values of the DC-side capacitor voltages for each bridge, as shown in Table 3.

Table 3 Modified modulation regions for u_{con}

Partition	u_{con} *and is symbols are the same*	u_{con} *and* i_s *symbols are opposite*
Region 1	$0 \le u_{con} < u_{dc1}$	$0 \le u_{con} < u_{dc4}$
Region 2	$u_{dc1} \le u_{con} < (u_{dc2} + u_{dc1})$	$u_{dc4} \le u_{con} < (u_{dc4} + u_{dc3})$
Region 3	$(u_{dc2} + u_{dc1}) \le u_{con} < (u_{dc3} + u_{dc2} + u_{dc1})$	$(u_{dc4} + u_{dc3}) \le u_{con} < (u_{dc4} + u_{dc3} + u_{dc2})$
Region 4	$(u_{dc3} + u_{dc2} + u_{dc1}) \le u_{con} < (u_{dc4} + u_{dc3} + u_{dc2} + u_{dc1})$	$(u_{dc4} + u_{dc3} + u_{dc2}) \le u_{con} < (u_{dc4} + u_{dc3} + u_{dc2} + u_{dc1})$
Region – 1	$-u_{dc1} \le u_{con} < 0$	$-u_{dc4} \le u_{con} < 0$
Region – 2	$-(u_{dc2} + u_{dc1}) \le u_{con} < -u_{dc1}$	$-(u_{dc4} + u_{dc3}) \le u_{con} < -u_{dc4}$
Region – 3	$-(u_{dc3} + u_{dc2} + u_{dc1}) \le u_{con} < -(u_{dc2} + u_{dc1})$	$-(u_{dc4} + u_{dc3} + u_{dc2}) \le u_{con} < -(u_{dc4} + u_{dc3})$
Region – 4	$-(u_{dc4} + u_{dc3} + u_{dc2} + u_{dc1}) \le u_{con} < -(u_{dc3} + u_{dc2} + u_{dc1})$	$-(u_{dc4} + u_{dc3} + u_{dc2} + u_{dc1}) \le u_{con} < -(u_{dc4} + u_{dc3} + u_{dc2})$

(2) The light load assumption. The assumption in references [8, 9] is established under the condition of light load, where $u_s \approx u_{con}$, and u_{con} is synthesized using u_s as the modulation waveform. However, in practical scenarios, there may exist a certain phase difference between u_s and u_{con}. This contradiction between the assumption and the phase difference becomes evident under heavy load conditions. Therefore, it is necessary to synthesize u_{con} using the modulation waveform calculated based on the control strategy to address this issue.

(3) Balance speed and load imbalance level. Under light load conditions, where u_{con} has the same sign as i_s, it can be analyzed that the balance speed and load imbalance level of the fast balancing modulation trajectory based on two-dimensional modulation are inferior to the super-fast balancing modulation trajectory. Under heavy load conditions, the choice of Table 1 or Table 2 based on the sign relationship between u_{con} and is i_s equivalent to adjusting the angle between the output voltage waveform of each bridge and the inductor current i_s. Although this adjustment ensures stable operation of the rectifier system within a working region, compared to the modified super-fast balancing modulation trajectory, this adjustment method cannot guarantee that H-bridge 1 absorbs the maximum active power and H-bridge 4 releases the maximum active power. In other words, the multi-bridge cascade extension described in references [6, 8] is not the optimal solution in terms of balance speed and load imbalance level.

The cascade extension and optimization of multi-H-bridge inverter based on two-dimensional modulation

The extension proposed in references [4, 10] provides insights into the multi-dimensional modulation approach for cascaded H-bridge topologies. Based on different modulation regions, the corresponding H-bridges with the appropriate DC-side voltage sequence are selected (after sorting the DC-side capacitor voltages). This selection ensures that each H-bridge operates in either the "PWM" state or " -PWM" state within its respective modulation region. As a result, the multi-dimensional modulation is transformed into a two-dimensional modulation across pairs of bridges.

Due to the cascaded nature of multiple bridges, the two-dimensional modulation strategy can have an impact on the H-bridges that are not involved in the two-dimensional modulation. Therefore, it is necessary to establish optimization principles

Table 4 Operation states of H-bridges of CHBR in different regions based on super fast balance modulation cure when u_{con} and i_s have same signs

Partition	*H-bridge 1*	*H-bridge 2*	*H-bridge 3*	*H-bridge 4*
Region 1	1	1	-PWM	-1
Region 2	1	1	PWM	-1
Region 3	1	1	1	-PWM
Region 4	1	1	1	PWM
Region -1	-1	-1	PWM	1
Region -2	-1	-1	-PWM	1
Region -3	-1	-1	-1	PWM
Region -4	-1	-1	-1	-PWM

Table 5 Operation states of H-bridges of CHBR in different regions based on super fast balance modulation cure when u_{con} and i_s have opposite signs

Partition	*H-bridge 1*	*H-bridge 2*	*H-bridge 3*	*H-bridge 4*
Region 1	-1	-PWM	1	1
Region 2	-1	PWM	1	1
Region 3	-PWM	1	1	1
Region 4	PWM	1	1	1
Region -1	1	PWM	-1	-1
Region -2	1	-PWM	-1	-1
Region -3	PWM	-1	-1	-1
Region -4	-PWM	-1	-1	-1

among the bridges: ensuring that the bridge with the lowest DC-side capacitor voltage receives the highest amount of active power compared to the other bridges, and the bridge with the highest capacitor voltage receives the least amount of active power relative to the other bridges. Priority should be given to charging the bridge with the lowest voltage and discharging the bridge with the highest voltage, followed by charging the bridge with the second-lowest voltage and discharging the bridge with the second-highest voltage, and so on. The bridge with an intermediate voltage level has the lowest priority.

Based on the optimization logic described above, if we simply incorporate the super-fast balancing modulation trajectory from two-dimensional modulation into Tables 1 and 2, we obtain Tables 4 and 5. In Table 4, H-bridge 2 and H-bridge 3 utilize the two-dimensional modulation super-fast balancing modulation trajectory in Region 1, Region 2, Region -1, and Region -2. Similarly, H-Bridge 1 and H-Bridge 4 employ the two-dimensional modulation super-fast balancing modulation trajectory in Region 3, Region 4, Region -3, and Region -4. The interrelationships between the bridges can be derived from Table 5. Based on the results in Tables 4 and 5, we can determine the new modulation partitions as shown in Table 6.

Based on the analysis results in Table 6, when u_{con} and i_s have the same sign and u_{con} is in Region 1, in order to synthesize the corresponding stepped waveform, the voltage relationships among the bridges need to meet:

Table 6 Modulation partition of u_{con} based on the modified super-fast balancing trajectory with a stepped waveform stacking method

Partition	u_{con} *and is symbols are the same*	u_{con} *and* i_s *symbols are opposite*
Region 1	$0 \le u_{con} < (u_{dc1} + u_{dc2}\text{-}u_{dc4})$	$0 \le u_{con} < (u_{dc4} + u_{dc3}\text{-}u_{dc1})$
Region 2	$(u_{dc1} + u_{dc2}\text{-}u_{dc4}) \le u_{con} < (u_{dc1} + u_{dc2} + u_{dc3}\text{-}u_{dc4})$	$(u_{dc4} + u_{dc3}\text{-}u_{dc1}) \le u_{con} < (u_{dc4} + u_{dc3} + u_{dc2}\text{-}u_{dc1})$
Region 3	$(u_{dc1} + u_{dc2} + u_{dc3}\text{-}u_{dc4}) \le u_{con} < (u_{dc1} + u_{dc2} + u_{dc3})$	$(u_{dc4} + u_{dc3} + u_{dc2}\text{-}u_{dc1}) \le u_{con} < (u_{dc4} + u_{dc3} + u_{dc2})$
Region 4	$(u_{dc1} + u_{dc2} + u_{dc3}) \le u_{con} < (u_{dc1} + u_{dc2} + u_{dc3} + u_{dc4})$	$(u_{dc4} + u_{dc3} + u_{dc2}) \le u_{con} < (u_{dc4} + u_{dc3} + u_{dc2} + u_{dc1})$
Region − 1	$\text{-}(u_{dc1} + u_{dc2}\text{-}u_{dc4}) \le u_{con} < 0$	$\text{-}(u_{dc4} + u_{dc3}\text{-}u_{dc1}) \le u_{con} < 0$
Region − 2	$\text{-}(u_{dc1} + u_{dc2} + u_{dc3}\text{-}u_{dc4}) \le u_{con} < \text{-}(u_{dc1} + u_{dc2}\text{-}u_{dc4})$	$\text{-}(u_{dc4} + u_{dc3} + u_{dc2}\text{-}u_{dc1}) \le u_{con} < \text{-}(u_{dc4} + u_{dc3}\text{-}u_{dc1})$
Region − 3	$\text{-}(u_{dc1} + u_{dc2} + u_{dc3}) \le u_{con} < \text{-}(u_{dc1} + u_{dc2} + u_{dc3}\text{-}u_{dc4})$	$\text{-}(u_{dc4} + u_{dc3} + u_{dc2}) \le u_{con} < \text{-}(u_{dc4} + u_{dc3} + u_{dc2}\text{-}u_{dc1})$
Region − 4	$\text{-}(u_{dc1} + u_{dc2} + u_{dc3} + u_{dc4}) \le u_{con} < \text{-}(u_{dc1} + u_{dc2} + u_{dc3})$	$\text{-}(u_{dc4} + u_{dc3} + u_{dc2} + u_{dc1}) \le u_{con} < \text{-}(u_{dc4} + u_{dc3} + u_{dc2})$

$$u_{dc3} \ge u_{dc1} + u_{dc2} - u_{dc4} \tag{2}$$

$$u_{dc1} + u_{dc2} - u_{dc4} \ge 0 \tag{3}$$

Furthermore, due to the system satisfying $u_{dc1} \le u_{dc2} \le u_{dc3} \le u_{dc4}$, Eq. (2) naturally holds, while Eq. (3) may not hold. When u_{con} and is have opposite signs, and u_{con} is in Region 1, in order to synthesize the corresponding stepped waveform, the voltage relationships among the bridges need to satisfy:

$$u_{dc4} + u_{dc3} - u_{dc1} \ge 0 \tag{4}$$

$$u_{dc2} \ge u_{dc4} + u_{dc3} - u_{dc1} \tag{5}$$

It is evident that Eq. (4) naturally holds, while Eq. (5) will definitely not hold. This means that when u_{con} and i_s have opposite signs, there is a modulation failure phenomenon during the first step of the stacked stepped waveform. It is not possible to achieve perfect synthesis through this extension at the zero-crossing point of u_{con}.

Based on this observation, it can be seen that simply incorporating the stacked stepped waveform method to introduce the super-fast balancing modulation trajectory of two-dimensional modulation into multi-H-bridge cascaded modulation will increase the system's restrictive conditions and result in modulation failure. Therefore, this method is not advisable.

In order for the system to operate stably, the rectifier stage must operate within a stable operating region. When performing two-dimensional modulation with a cascade of two H-bridges, any chosen modulation trajectory within the two-dimensional modulation region can be used, ensuring that the system operates in a stable working region. Therefore, starting from the perspective of the system's stable working region, we ensure that the bridge with the lowest DC-side voltage operates within its stable working point in conjunction with the other bridges. Then, we determine the working points for the bridge with the second-lowest voltage and the remaining bridges, excluding the one with the lowest voltage. This process is repeated, ultimately determining the working points for each bridge within the stable working region. Figure 4 depicts the determination of the working points for each bridge based on the modified super-fast modulation trajectory in the context of two-dimensional modulation. This approach transforms the

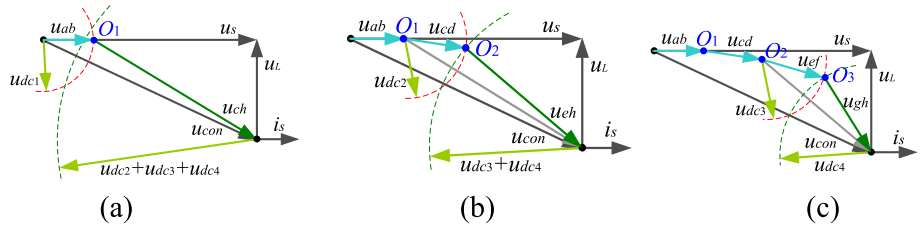


Fig. 4 The choosing method of operation points for four H-bridges of CHBR. **a** The choice of operation point of H-bridge 1. **b** The choice of operation point of H-bridge 2. **c** The choices of operation points of H-bridge 3 and H-bridge 4

Table 7 Simulation parameters

Parameter name	*Parameter value*	*Parameter name*	*Parameter value*
Power supply voltage u_s peak/frequency	310 V/50 Hz	H-bridge 1 load *R1*	120Ω
Filter inductance *L*	10mH	H-bridge2 load *R2* before change	150Ω
The DC-side capacitance *C* of each bridge is equal	2200*μF*	H-bridge2 load *R2* after change	280Ω
DC side command voltage u_{dc}*	80 V	H-bridge3 load *R3*	110Ω
Switching frequency	2 kHz	H-bridge3 load *R3*	130Ω
Voltage loop K_P/K_I	0.2/12	Current loopK_P/K_I	1200/0

u_{dc}* is the command voltage on the DC side of a single H-bridge

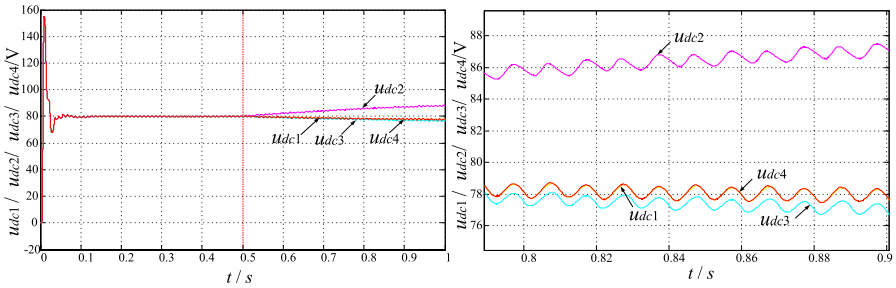
problem of multi-bridge cascaded modulation into a two-dimensional modulation problem, allowing the smooth transfer of various optimized modulation trajectories within the two-dimensional modulation framework.

Extension and optimization of cascaded rectifier stages using a multi-H-bridge configuration based on two-dimensional modulation

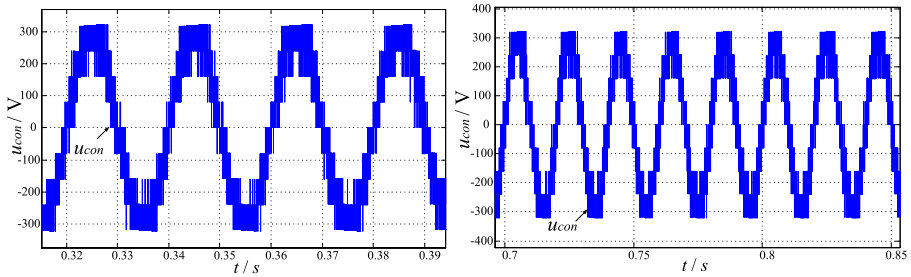
To validate the feasibility of the proposed control scheme, simulation studies were conducted. First, typical methods for centralized and decentralized control structures in a four-bridge cascaded configuration were simulated. Subsequently, comparative simulations were performed for the proposed extension and optimization of a four-H-bridge cascaded rectifier stage based on two-dimensional modulation. To ensure better comparability among the different control methods, the control section of the rectifier stage system employed a direct current method, with consistent PID parameters for the voltage and current loops. The simulation parameters for the four-bridge cascaded rectifier stage are listed in Table 7.

The typical centralized control structure adopts the control scheme shown in Fig. 1. The simulation was conducted for a duration of 4 s, and at $t=2$ s, the load R2 of H-bridge 2 abruptly changes to 280Ω. The simulation results are illustrated in Fig. 5.

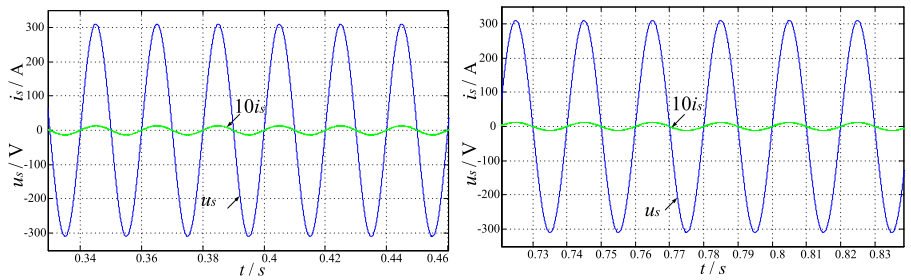
After system startup, the DC-side capacitor voltages of the cascaded H-bridges reach their initial balance at approximately 1.2 s. At 2 s, a sudden change occurs in R2, leading to increased load imbalance between the bridges. Since saturation limiters were not set for each independent voltage PI controller, the DC-side capacitor voltages of the bridges cannot continue to balance, as shown in Fig. 5a, b. Before the load mutation,



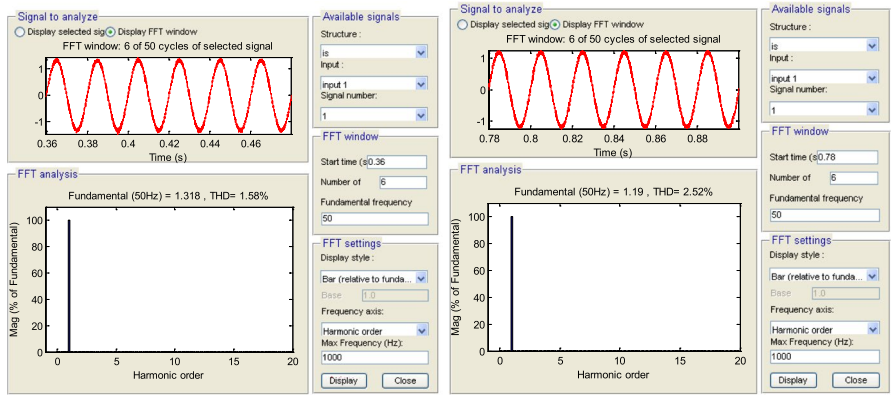
(a)DC link voltages of CHB (b)DC link voltages of CHB after R_2 changed



(c) The output waveform of CHBR in its AC-side before load changed (d) The output waveform of CHBR in its AC-side after load changed



(e) Source voltage and inductor current before load changed (f) Source voltage and inductor current after load changed



(g) FFT analysis of inductor current before load changed (h) FFT analysis of inductor current after load changed

Fig. 5 Simulation results of CHBR with four cells based on centralized control structure. **a** DC link voltages of CHB. **b** DC link voltages of CHB after R_2 changed. **c** The output waveform of CHBR in its AC-side before the load changed. **d** The output waveform of CHBR in its AC-side after load changed. **e** Source voltage and inductor current before load changed. **f** Source voltage and inductor current after load changed. **g** FFT analysis of inductor current before load changed. **h** FFT analysis of inductor current after load changed

the modulation section adopts the standard phase-shifted carrier-based method. After the DC-side capacitor voltages of the bridges are balanced, the rectifier stage system outputs a standard nine-level stepped waveform on the AC side, as shown in Fig. 5c. However, after the load mutation, the DC-side capacitor voltages of the bridges cannot maintain balance, resulting in increased harmonic distortion in the synthesized stepped waveform, as depicted in Fig. 5d. Consequently, the waveform of the inductor current also deteriorates, and the total harmonic distortion (THD) increases from the original 7.67% to 40.09%, as shown in Fig. 5g, h. Despite the load mutation, the phase relationship between the power supply voltage and the inductor current remains unchanged, allowing the system to maintain a relatively good power factor operating state.

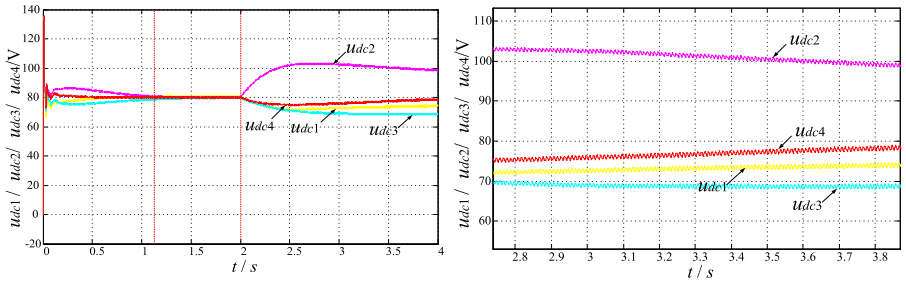
The modified simulation results for the decentralized control structure proposed in references [9, 10] are shown in Fig. 6. The simulation was performed for a duration of 1 s, and at $t=0.5$ s, the load R2 of H-bridge 2 experienced a sudden change.

Compared to the centralized control structure, decentralized control integrates the balancing and modulation components together. The balancing strategy adopts a comparative exchange approach. This balancing method utilizes independent voltage PI controllers with different saturation upper and lower limits, resulting in a significantly faster balancing speed compared to the centralized control structure. During the system startup process, the DC-side capacitor voltages of each bridge remain balanced, as shown in Fig. 6a. At 0.5 s, due to the load mutation, in order to maintain unity power factor operation, the modulation strategy from references [4, 5] is allocated to the bridge with the lightest load, where its functional quantity is greater than the load consumption. As a result, the DC-side capacitor voltage of H-bridge 2 increases while the other bridge's capacitor voltages decrease. The DC-side capacitor voltages of the bridges cannot continue to balance, as illustrated in Fig. 6b. Before and after the load mutation, the rectifier stage system outputs a nine-level stepped waveform on the AC side, consistently ensuring unity power operation, as shown in Fig. 6c–f. Due to the load mutation, the DC-side capacitor voltages of the bridges do not exhibit significant oscillations as observed in the centralized structure. Therefore, the harmonic content of the inductor current does not increase significantly, as depicted in Fig. 6g, h.

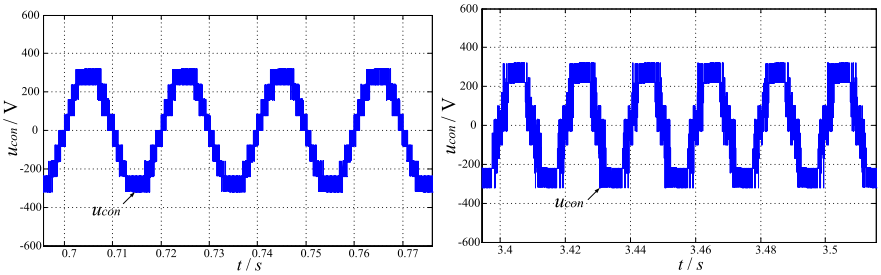
In the following simulation study, the proposed method for cascaded rectifiers with multi-H bridges is examined using a modified two-dimensional modulation-based ultrafast balancing modulation trajectory. It gradually searches for the fastest capacitor voltage balancing speed for each bridge in the stable operating region, as shown in Fig. 4. The bridge activation method is inspired by the concept of phase-shifted carrier, where the PWM counters operate in a continuous increment-decrement counting mode, as depicted in Fig. 7. Each bridge counter is mutually incorrect, with N representing the number of cascaded H-bridges. All bridges employ the activation method illustrated in Fig. 7a. The simulation time for the system is 1 s, and at $t=0.5$ s, there is a sudden change in load R2 of H-bridge 2. The simulation results are shown in Fig. 7.

To verify the above theory, our research group has built an experimental platform for a three-phase cascade rectifier stage system using TMS320F2812 as the controller, as shown in Fig. 8.

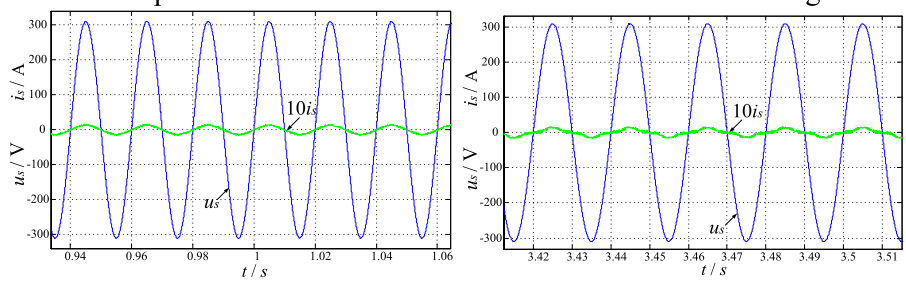
(1) Modulation strategy inversion experiment



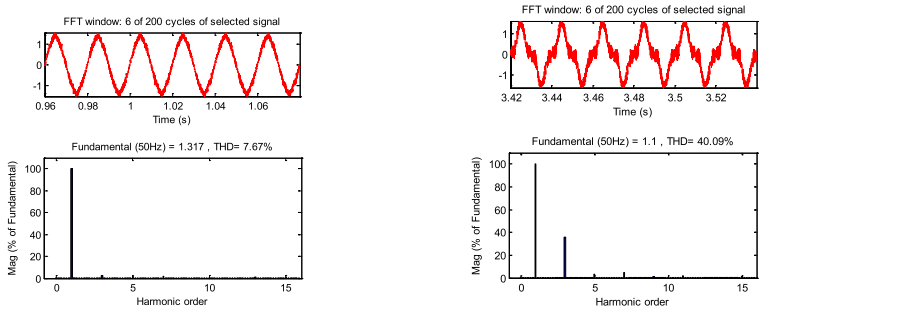
(a)DC link voltages of CHB (b)DC link voltages of CHB after R2 changed



(c)The output waveform of CHBR in its AC side before load changed (d) The output waveform of CHBR in its AC side after load changed

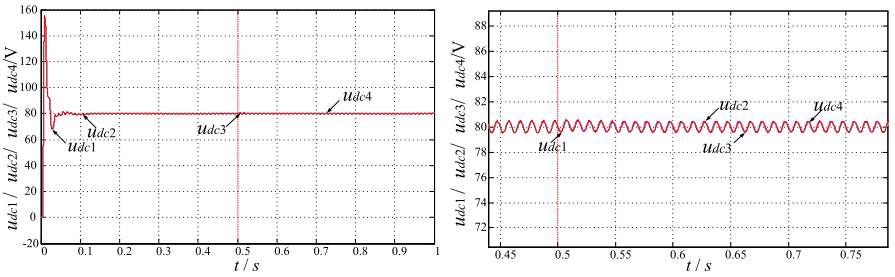


(e) Source voltage and inductor current before load changed (f) Source voltage and inductor current after load changed

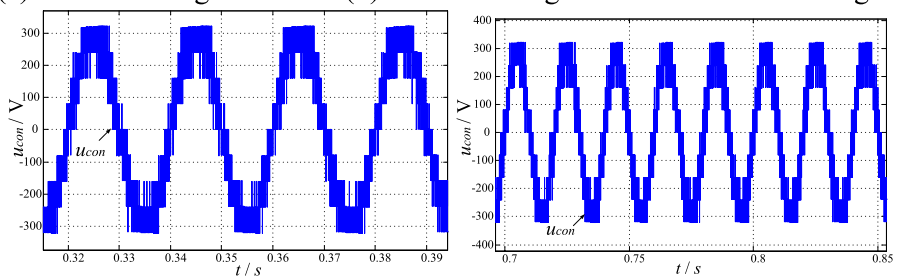


(g) FFT analysis of inductor current before Load changed (h) FFT analysis of inductor current after load changed

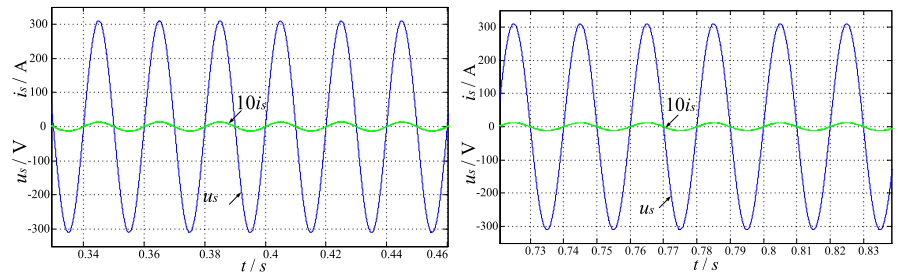
Fig. 6 Simulation results of CHBR with four cells based on distributed control structure. **a** DC link voltages of CHB. **b** DC link voltages of CHB after R2 changed. **c** The output waveform of CHBR in its AC side before load changed. **d** The output waveform of CHBR in its AC side after load changed. **e** Source voltage and inductor current before load changed. **f** Source voltage and inductor current after load changed. **g** FFT analysis of inductor current before Load changed. **h** FFT analysis of inductor current after load changed



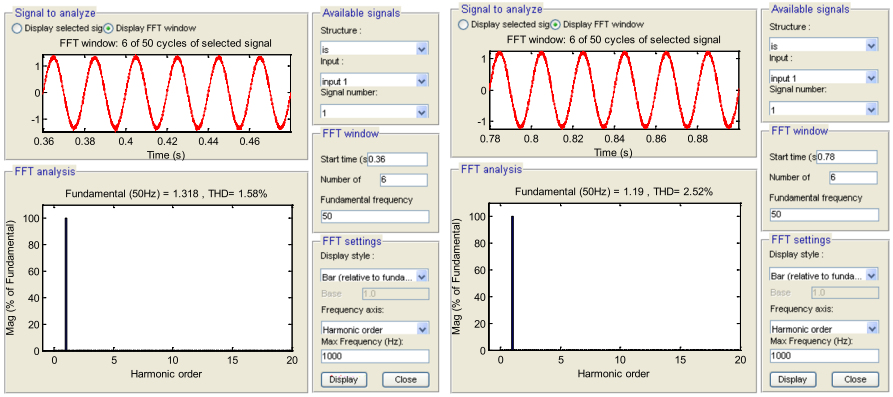
(a)DC link voltages of CHB (b)DC link voltages of CHB after R_2 changed



(c) The output waveform of CHBR in its AC-side before load changed (d) The output waveform of CHBR in its AC-side after load changed



(e) Source voltage and inductor current before load changed (f) Source voltage and inductor current after load changed



(g) FFT analysis of inductor current before load changed (h) FFT analysis of inductor current after load changed

Fig. 7 Simulation results of CHBR extension based on modified super fast balance modulation curve. **a** DC link voltages of CHB. **b** DC link voltages of CHB after R_2 changed. **c** The output waveform of CHBR in its AC-side before load changed. **d** The output waveform of CHBR in its AC-side after load changed. **e** Source voltage and inductor current before load changed. **f** Source voltage and inductor current after load changed. **g** FFT analysis of inductor current before load changed. **h** FFT analysis of inductor current after load changed

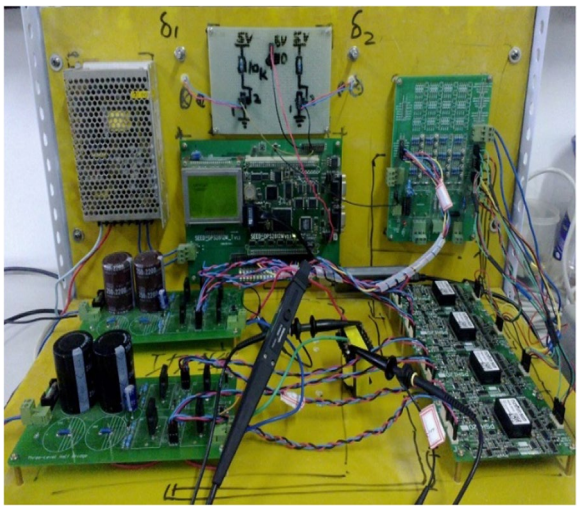


Fig. 8 Transformer system experimental platform

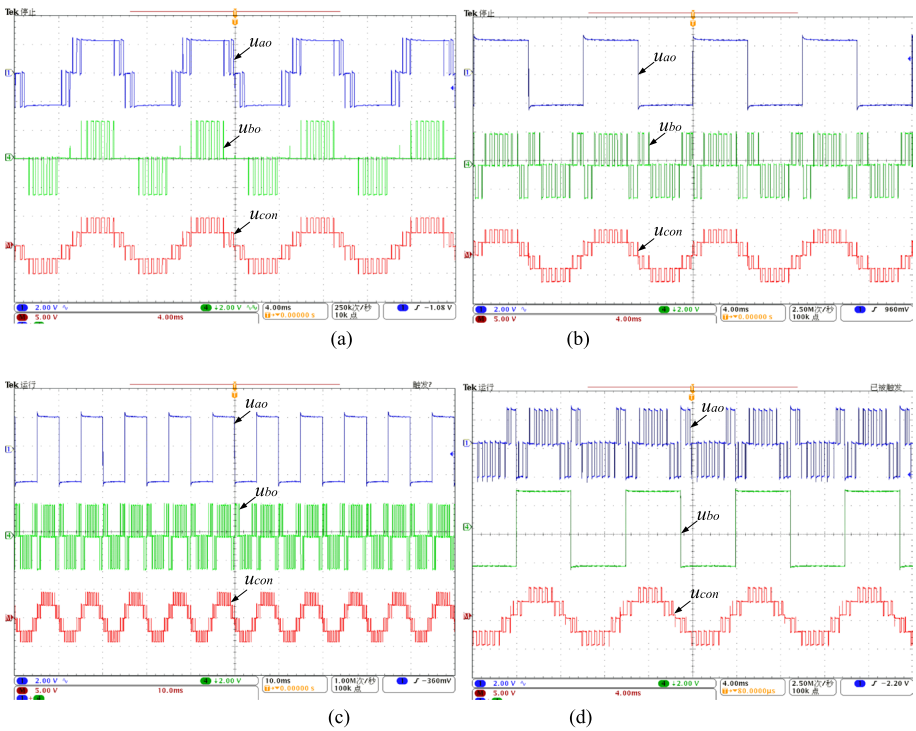


Fig. 9 The AC output waveform of CHB inverter

Prior to the rectification test, the two-bridge modulation method is first validated. An inverter is used to apply a 23 V DC voltage to the DC side of H-bridge 1 and a 26 V DC voltage to the DC side of H-bridge 2. The synthesized ucon is a sinusoidal voltage with an amplitude of 40 V. The experimental results of the inverter are shown in Fig. 9.

Figure 9a shows the output waveform and synthesized waveform of the two bridges using fast balance modulation trajectory modulation; Fig. 9b shows the output waveform and synthesized waveform of the two bridges using ultra-fast balanced modulation

trajectory modulation; When u_{con} and i_s are in the same direction in Fig. 9c, the two bridge output waveform and composite waveform are modulated using the modified ultra fast balance modulation trajectory. When u_{con} and i_s are in the opposite direction in Fig. 9c, the two bridge output waveform and composite waveform are modulated using the modified ultra-fast balance modulation trajectory.

(2) Cascade rectifier stage steady-state operation rectifier experiment

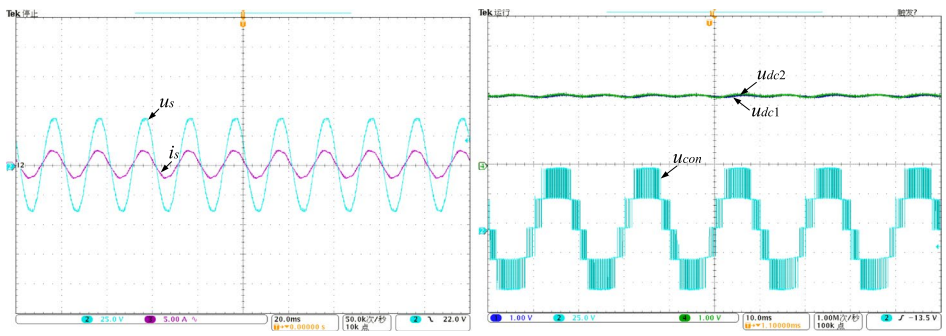
After the rectification system stabilizes, several balanced modulation trajectory modulation based on two-dimensional modulation can achieve unit power factor operation of the rectification stage, as shown in Fig. 10a. Within the limiting range of load imbalance, it is possible to achieve voltage balance between the DC side capacitors of two cascaded H-bridges, while outputting a 2n + 1 step wave on the AC side of the rectifier stage, as shown in Fig. 10b.

(3) Experiment on the degree of load imbalance in different balanced modulation strategies

The verification of the degree of load imbalance for three balanced modulation strategies is shown in Fig. 11. When the rectifier stage load R_2 using fast balance modulation trajectory modulation becomes 210 Ω, the DC side capacitor voltage cannot be rebalanced, as shown in Fig. 11a. The rectifier stage using ultra-fast balance modulation trajectory modulation (as shown in Fig. 11b) and modified ultra fast balance modulation trajectory modulation (as shown in Fig. 11c) maintains balance in the DC capacitor voltage even after the same change in load. Due to the relatively light load, the difference in load imbalance range between the ultra-fast balance modulation trajectory modulation and the corrected ultra-fast balance modulation trajectory modulation is relatively small.

(4) Experiment of equilibrium velocity of different equilibrium modulation strategies

Firstly the load R_2 is set to 250 Ω, and at a certain moment it is set to 100 Ω, other test parameters are shown in Table 8. The experimental results of three balanced modulation strategies are shown in Fig. 12. The recovery time of the DC side capacitor voltage of the



(a) (b)

Fig. 10 The steady-state waveform of cascade rectifier

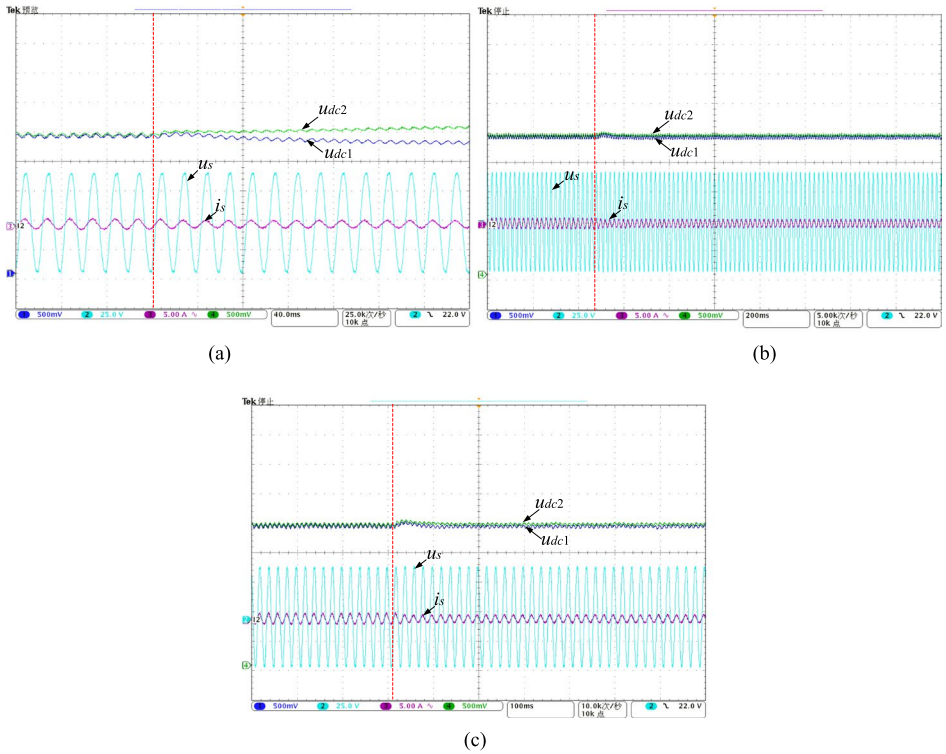


Fig. 11 The waveform of the cascade rectifier in case of load abrupt change

Table 8 Experiment parameters

Parameter name	*Parameter value*	*Parameter name*	*Parameter value*
Power supply voltage u_s peak/frequency	40V/50 Hz	Filter inductance L	10 mH
The DC side capacitance $C_1 = C_2$	2200 μF	DC side command voltage u_{dc}*	25 V
Switching frequency	2 kHz	Load R_2 of H-bridge2 before 0.5s	100 Ω
Load R_1 of H-bridge1	70 Ω	Load R_2 of H-bridge2 after 0.5 s	210 Ω

u_{dc}* is the command voltage on the DC side of a single H-bridge

rectifier stage using fast balance modulation trajectory modulation is 147 ms, as shown in Fig. 12a. The recovery time of the DC side capacitor voltage of the rectifier stage using ultra-fast balanced modulation trajectory modulation is 90 ms, as shown in Fig. 12b. The recovery time of the DC side capacitor voltage of the rectifier stage modulated by the modified ultra fast balance modulation trajectory is 80 ms, as shown in Fig. 12c. At the same time, it can be seen that under the same load difference, the difference in DC capacitor voltage between the two cascaded H-bridges is also different when using different balanced modulation strategies.

Results

From Figs. 7, 8, 9, 10, 11, and 12, it can be observed that the extended approach proposed in this paper successfully transfers the advantages of the two-dimensional modulation-based ultra-fast balancing modulation trajectory to the multi-bridge cascaded

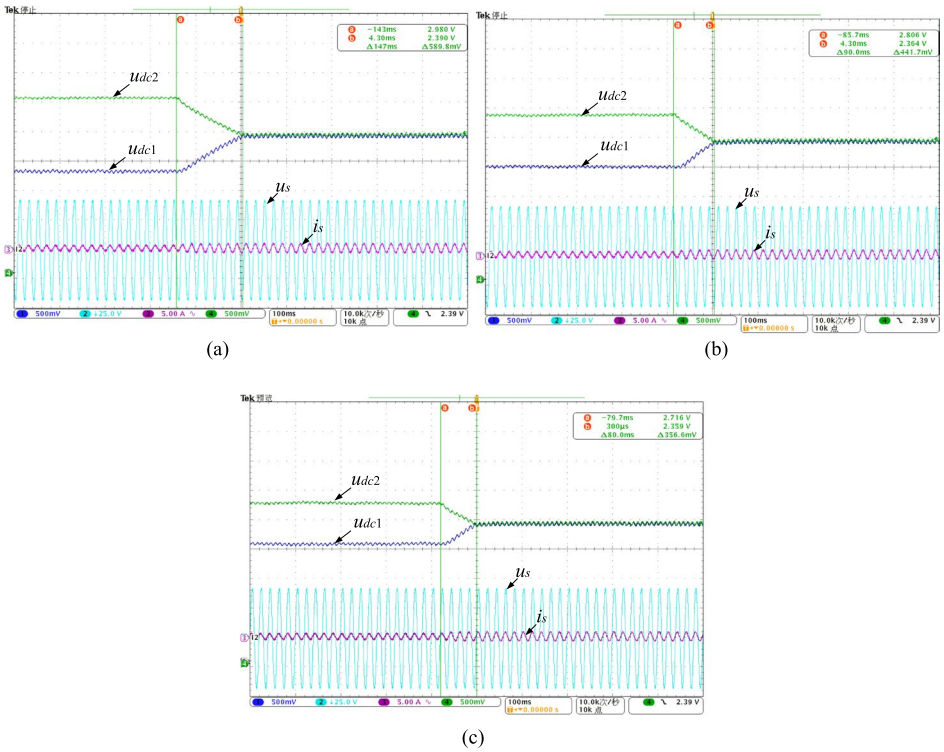


Fig. 12 The voltage balance speed waveform of CHBR under different loads

rectifier system. The DC-side capacitor voltages of the four H-bridges remain well-balanced before and after the load mutation. Since the simulations with the modified decentralized control structure, as proposed in references [7, 9], utilizing the same PI parameters, the overshoot, and oscillation of the DC-side voltages during system startup are consistent in both scenarios. Similar to the constraints analyzed for load imbalance in a two-bridge cascaded configuration, the extended approach presented in this paper effectively expands the degree of load imbalance while ensuring unity power factor operation. Due to the continuous balance of the capacitor voltages across the bridges, the synthesized nine-level stepped waveform exhibits low harmonic content, resulting in a total harmonic distortion (THD) of the inductor current below 3%.

Discussion

(1) The common characteristic of both control structures is the requirement of an overall voltage control loop. The main difference lies in whether each cascaded H-bridge has an independent voltage loop. Therefore, the core of the centralized control structure is the extension of independent PI voltage loops, while the core of the decentralized control structure is the extension of a multi-level staircase waveform synthesis method.

(2) The multi-bridge cascade extension described in references [7, 8] corresponds to the two-dimensional modulation's fast-balancing modulation trajectories. Each step of the synthesized multi-level staircase waveform is the result of the interaction

between two bridges in the corresponding order of DC-side voltage magnitudes, while the other bridges select fixed operating states based on the magnitude of the DC-side voltages and the requirements of the staircase waveform. This process is repeated, continuously sorting, exchanging modulation waves, and transitioning operating states within each switching cycle to ultimately achieve the balance of the DC-side capacitor voltages of each bridge.

(3) To validate the feasibility of the proposed control scheme, simulation studies were conducted. First, typical methods for centralized and decentralized control structures in a four-bridge cascaded configuration were simulated. Subsequently, comparative simulations were performed for the proposed extension and optimization of a four-H-bridge cascaded rectifier stage based on two-dimensional modulation. However, in practical applications, the impact of parameter errors on system performance should also be considered.

(4) From Figs. 9, 10, 11, and 12, the order of voltage differences among the three balance modulation strategies is: the DC side voltage difference of the fast balance modulation trajectory modulation is greater than that of the ultra-fast balance modulation trajectory modulation, while the voltage difference of the modified ultra fast balance modulation trajectory modulation is the smallest. This also verifies that using the modified ultra-fast balance trajectory is the most functional quantity that can be allocated to the H-bridge with lower DC side voltage among the three balance modulation strategies. The experimental results are consistent with the simulation results, which further verify the superiority of using the modified ultra-fast balance modulation trajectory modulation.

Conclusions

Based on the analysis of two control structures for balancing the capacitor voltages in cascaded rectifier stages, this paper proposes a cascaded rectifier multi-H-bridge extension and optimization control strategy based on two-dimensional modulation. Through simulation studies, it is found that in the case of traditional control methods applied to both centralized and decentralized control structures of four-bridge cascaded systems, the capacitor voltages on the DC side cannot maintain balance after a load disturbance, resulting in increased harmonic content of the synthesized stepped waveform and deteriorated waveform of the inductor current. The total harmonic distortion (THD) increases from 7.67 to 40.09%. By using the proposed cascaded rectifier multi-H-bridge extension and optimization method with modified two-dimensional modulation and fast-balancing modulation trajectory, the simulation study achieves fast-tracking of the most rapidly balancing operating points for the capacitor voltages in the stable operating region. This ensures a continuous balance of the capacitor voltages across all bridges, reduces the harmonic content of the synthesized nine-level stepped waveform and keeps the THD of the inductor current below 3%. Therefore, this method provides a highly reliable and effective approach for cascaded rectifier multi-H-bridge extension. However, in practical applications, the impact of parameter errors on system performance should also be considered.

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Author's contributions
Jingpeng Hu fully contributed to the manuscript. The author read and approved the final manuscript.

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Availability of data and materials
The data used to support the findings of this study are included in the article.

Declarations

Competing interests
The author declares no competing interests.

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