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Performance evaluation of hybrid multilevel inverter with a high-frequency switching technique

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Abstract

This proposed work deals with the implementation of a single-phase topology with using hybrid for multilevel inverters. It is observed that the proposed structure improves the performance of the hybrid multilevel inverter with high-frequency switches for positive levels and reverse voltage with negative levels. This paper studies a novel construction for an asymmetrical hybrid single-phase multilevel inverter. This paper also studies the operation of multi level inverter under depreciating sources condition due to fluctuation in input. The PWM method, i.e. APOD and CO, has been incorporated into the simulation of single-phase 7-level, 9-level, and the 11-level hybrid inverter. These two methods are compared to one another and to standard methods in terms of THD for different values of the modulation index, and they are found to be superior. Overall loss of 50% of the THD is almost equal to rated output voltage, it is observed in cascaded multilevel inverters. The working and performance of the proposed model are simulated in MATLAB Simulink software and the results are discussed in detail.

Keywords: Cascaded hybrid multilevel inverter, THD, Inverter, Pulse width modulation, Performance

Introduction

The development of power electronics and switching devices yielded to development of multilevel inverters and their appropriateness for grid connections. There is a different kind of multilevel inverters having diversity in their operation [1–4]. From the power converter technology, the structures access the alliance of renewable energy systems for power generation. So, the researchers have more attention in this field to develop various topologies with different switching patterns to reduce part count as well as system performance improvement. In this connection cascaded multilevel inverters with a connection of input voltage sources to reach high-quality output voltage, input currents. So, in the power sector in the medium voltage range cascaded multi-level inverters (MLIs) substitute other trends [5, 6].

Recently a variety of modulation strategies are encountered in multilevel inverters. Because of advancements in multilevel inverters spreading in all corners of the power

electronics and control applications such as electric drives, renewable energy access to micro grid and flexible AC transmission systems, etc. Even though they are used in a wide variety of applications some of the facts made them limitations like more number of semiconductor devices are needed when voltages levels are increased, so it is required to maintain less amount of switch count [7, 8].

In high power applications, hybrid multilevel inverters are more useful where some of the switches are operated at switching with lower voltage frequencies while continuing to run at higher line frequencies. Integration of half and full-bridge hybrid inverters have to produce seven output levels this concept is also utilized in this proposed structure [9]. Present development in distributed power generation along with non-conventional sources, the researchers has attention on-grid interfacing. This proposed structure is designed for the most suitable grid interfacing, the controlling strategy of current injection and suppressing dc current to the grid is more and dc offset is a problem in facing when attaching solar inverters to a grid [10].

For a high-power application, a multilayer converter system may be readily interfaced with renewable energy resources including wind, solar and fuel cells. Modern research has focused on original modulation techniques and innovative converter topologies. Three distinct primary multilevel inverters topologies have also been documented in the survey: cascaded H-bridges converter with independent dc sources, flying capacitors and neutral clamped. In addition, several control paradigms and modulation approaches have been created for multilevel converters [11]. The most recent multilayer inverter (MLI) development is using medium voltages in industrial drives to supply power up to several megawatts. For high power applications in the power industry, MLI technologies are attracting more attention. This is because the output waveforms are better than they were for two level inverters. To create ac output waveforms, the inverter's bipolar transistor (BJT), insulated gate transistor (IGBT), and metal oxide semiconductor (MOSFET) switches are switched on and off in the precise order dictated by the modulation (PWM) technique [12].

The idea behind power conversion in multilevel inverters (MLI) is to create a staircase waveform from a number of low-voltage DC sources that is closer to a sinusoidal wave with less harmonic distortion. This concept has a number of benefits and has generated a lot of interest in high power, high voltage applications. The semiconductors are connected in series type for multilayer inverters so that operation at greater voltages is feasible. Because the switches are not really linked in series, the switching losses and frequency can be decreased via staggered switching. Traditional multilevel inverters include the cascaded H- bridge inverter, flying capacitor (capacitor clamped), and neutral point clamped (diode-clamped) inverters [13]. The requirement for a greater number of power semiconductor switches, which complicates the entire system, is the main disadvantage of multilayer inverter. In comparison to two level inverters, the cost of active semiconductors can be decreased by using switches with lower ratings in multilayer inverters. Each active semiconductor has an associated gate drive circuit, which adds to the complexity. Recent study [14] discusses reversing voltage architecture for multiple inverters. Comparing this multilevel inverter architecture to traditional multilevel inverters, fewer components are needed. When compared to traditional multilevel inverters, a multilevel inverter with a reversing voltage component offers significant benefits as the levels rise.

The hybrid topology minimises the switches and carrier signals needed compared to cascaded inverters, diode clamped inverters, and flying capacitor inverters. It also removes the diodes and capacitors used in diode clamped inverters and capacitors used in flying capacitor inverters. Utilising high-power devices with low switching frequencies minimises output voltage distortion, but has current harmonics, which is a significant disadvantage. There are asymmetrical ways to use several voltage sources, which call for more power switches and diodes with various ratings. Problems with capacitor balance affect several topologies. As opposed to the approaches outlined above, a hybrid multilevel inverter uses voltage sources with equal values and has various advantages [15]. It is more efficient because it employs fewer switches, fewer carrier waves, and switches that operate at line frequency. It has been suggested that a variety of carrier-based PWM approaches can reduce total harmonic distortion (THD). Recently, advanced multilevel inverter topologies such the hybrid multilevel inverter, soft switching inverter, and generalised multilevel inverter have been presented. Applications including FACTS, tractions, and industrial drives have made substantial use of multilayer inverters. In this study, the inverter is driven using the phase disposition (PD), alternate phase opposition disposition (APOD), and carrier overlapping (CO) sinusoidal pulse width modulation (SPWM) approaches [16].

Multilevel converters (MLCs) have been more common in high-power applications during the past few decades. Their capacity to distribute the high-voltage strains among the devices, reduced conduction and switching losses, and enhanced power quality with little harmonic distortion are the causes of their broad popularity.

The converter must provide higher output voltage levels in order to improve the power quality to IEEE standards, which call for 5% current total harmonic distortion (THD). However, the higher output voltage level necessitates additional parts and floating capacitors, increasing the converter system's cost and size. Due to their low component count need, hybrid converter topologies, which combine traditional converters, have drawn a lot of interest from academics [17]. The hybrid converter decreases the need for component needs for the same output voltage levels by arranging different converters in a cascade. It might be difficult to keep hybrid multilevel inverters' (HMLIs') power quality up to par with industry requirements (IEEE-519). In recent decades, a variety of sophisticated control techniques have been created. A typical control technique in HMLIs is selective harmonic elimination pulse width modulation (SHE-PWM). The SHE-PWM provides effective switching losses management, although the complexity of the angle computation is increased by its modulation. Hybrid converters are subject to more sophisticated control methods, such as sinusoidal PWM (SPWM) and model predictive control (MPC) [9]. Due to its many benefits for MLCs, the MPC has been a promising control approach in business and academics for about three decades [18].

This control method is simple to implement and can readily incorporate nonlinear systems and restrictions. It also requires less sophisticated tuning. Additionally, the MPC does not need angular computation or reference voltage approximation methods, which lessens the complexity of its application in power electronic systems. Due to its straightforward and adaptable implementation, finite set model predictive control (FS-MPC) has gained appeal in power electronic systems [19]. Because FS-MPC is discrete, PWM is not required and it may be implemented directly. For regulating DC-DC and ACDC

converters, multilevel converters like packed U-cell (PUC) [9], and flying capacitor–based ANPC hybrid converters, the FS-MPC is extensively studied in the literature. The best control action among the finite control actions in the FS-MPC is obtained by solving an optimisation problem. To manage the switches of the multilayer converter and lower THD levels, nonlinear control techniques like sliding mode control (SML) are also utilised [20]. Better performance is provided by this resilient and dynamic architecture, but it is considerably more complicated and difficult to design and construct. This study analyses the circuit layout of the proposed hybrid multilevel inverter (HMLI), which is based on the series connection of an H-bridge converter and a cascaded converter module. Voltage and current controllers have been used as controllers, which are based on a simplified form of the HMLI.

The task is divided into two segments based on the controller design. The FS-MPC control approach is initially applied on the HMLI as a first control method for newly developed topology, and theoretical analysis is conducted in the MATLAB/Simulink environment. The suggested converter produces a nine-level output voltage with less current distortion using the FS-MPC approach. A hybrid control technique, a variation of the FS-MPC approach, has later been developed for the real-time implementation of the HMLI topology [21]. The HMLI topology has been used to operate the converter modules switches according to their voltage stresses since the proposed technique is computationally efficient. The cascaded converter module is controlled by FS-MPC, which optimally anticipates the next level, and the decision is applied by the pulse width modulation (PWM) technique. The H-bridge converter runs at fundamental switching frequency in the hybrid control scheme.

There are various benefits to the power conversion paradigm used in multilayer inverters. When compared to traditional multilevel inverters, a multilevel inverter with a reversing voltage component offers various benefits as the levels rise. The hybrid topology minimises the switches and carrier signals needed compared to cascaded inverters, diode clamped inverters, and flying capacitor inverters. It also removes the diodes and capacitors used in diode clamped inverters and capacitors used in flying capacitor inverters [22–24].

While a method of using high power devices with low switching frequency minimises output voltage distortion, it includes current harmonics, which is a significant disadvantage. There are asymmetrical ways to use diverse voltage sources, and these approaches call for additional power switches and diodes with various ratings, Capacitor balance issues affect some topologies. As opposed to the approaches outlined above, a hybrid multilevel inverter uses voltage sources with equal values and has various advantages. It is more efficient because it employs fewer switches, fewer carrier waves, and switches that operate at line frequency. In this study, the inverter is driven by alternating phase opposition disposition (APOD) and carrier overlapping (CO) sinusoidal pulse width modulation approaches [25, 26].

This paper is hereby proposing a new single-phase structure for hybrid multilevel inverters which has the optimum improvement in performance. Reducing the count of the components results in decay of power losses and increasing the system efficiency of the proposed topology. The proposed method uses a fewer number of components compared with the cascaded H-bridge and other conventional topologies. The working of the

inverter under varying operating points in the MATLAB/Simulink platform has been verified to explore the system performance of the proposed method.

Methodology

Dual input configuration with multi level inverter

The proposed schematic diagram is shown in Fig. 1; structurally this circuit consists of eight switches, located at two different hybrid bridges. Two isolated dc sources give (Vs1 and Vs2) supply to these two H- Bridges. V_{S2} is a voltage source of half of the V_{S1}. A new switching pattern is developed based on the logic-gate PWM technique. The switching pattern half of the switches operated at the fundamental frequency (50 Hz) therefore this is highly efficient. The proposed MLI structure developed as a single-phase cascaded hybrid bridge inverter as shown in Fig. 1.

Where Pm1, Pm2, Pm3, Pm4, Pm1b, Pm2b, Pm3b Pm4b are the gate pulses applied for the control circuit. The two-hybrid bridges are connected as cascaded to deliver a 7-level output voltage. Here in the proposed MLI half of the switches operated at fundamental frequency remaining at high frequency, in cascaded MLIs all operated at high frequency, this technique which is used is more efficient than cascaded MLIs.

The internal H- Bridge inverter source is half of the outside bridge voltage magnitude, so the voltages are $V_{S1} = 2V_{S2}$. This kind of isolated source is most useful for solar power generation and avoiding external balancing circuits for power balancing. This structure is very useful in extending the cascading more bridges to connect higher levels. The most advantage future in this structure if any inner bridge not working it can be bypassed, this technique is more useful in improving the reliability of the system.

Modulation strategy for suggested module

The proposed structure output voltage with seven levels like as ($3V_{S1}$, $-V_{S1}$, $-V_{S1}/2$, $V_{S1}/2$, V_{S1}, $3V_{S1}/2$). These are values synthesized in suitable steps for producing a

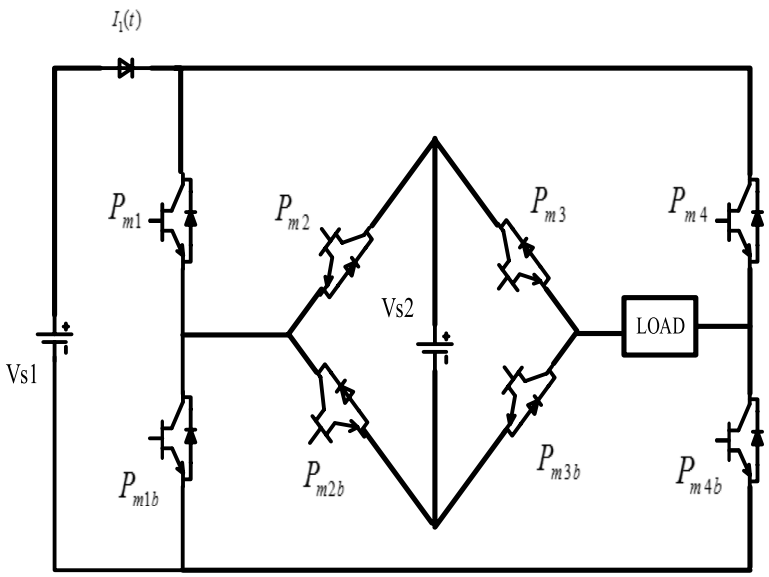

Fig. 1 Proposed single-phase inverter model

seven-level output voltage. The switching sequence is shown in Table 1. The table shows the switching sequence for the seven-level inverter, "0" indicating the switch is OFF and "1" indicating the switch is "ON". The operating of the switching sequence for producing each level is as follows.

From Fig. 2, the output positive voltage at maximum is obtained as (3 $V_{s1}/2$). From the figure observed that two sources added series and P_{m1}, P_{m3} from top position and P_{m2b}, P_{m4b} are from bottom half are chosen as ON, other switches are OFF. The load is integrated between the voltage terminals. A load voltage of $3V_{S1}/2$ is being used.

From Fig. 3, the output positive maximum voltage of 2/3 of V_{S1}. From observations P_{m1}, P_{m2}, P_{m4} from upper half portion of the circuit and P_{m3b} from lower half portion to operate the circuit, that is they are in ON position remaining all are in OFF position. Maximum voltage V_{S1} is applied across to the load.

From Fig. 4, the output positive maximum voltage of 1/3 of $V_{S1}/2$. From observations $P_{m1,}$ from upper half portion of the circuit and P_{m1b}, $P_{m2b}$and P_{m4b} from lower half portion to operate the circuit, that is they are in ON position remaining all are in OFF position. Maximum voltage $V_{S1}/2$ is applied across to the load.

From Fig. 5, the output of the circuit is zero. From observations lower half portion of the circuit and P_{m1b}, P_{m2b}, P_{m3b} and P_{m4b} to operate the circuit, that is they are in ON position remaining all are in OFF position. Maximum voltage is zero applied across to the load.

From Fig. 6, the output negative maximum voltage of 1/3 of ($-V_{S1}/2$). From observations P_{m3} from upper half portion of the circuit and P_{m1b}, $P_{m2b}$and P_{m4b} from lower half portion to operate the circuit, that is they are in ON position remaining all are in OFF position. Maximum voltage ($-V_{S1}/2$) is applied across to the load.

The operating modes of the proposed structure are as follows.

From Fig. 7, the negative maximum output voltage of 2/3 of ($-V_{S1}$). From observations $P_{m2,}$ P_{m3} and P_{m4} from upper half portion of the circuit and P_{m1b} from lower half portion to operate the circuit, that is they are in ON position remaining all are in OFF position. Maximum voltage (V_{S1}) is applied across to the load.

From Fig. 8, the negative maximum output voltage of $-3V_{S1}/2$. From observations P_{m2}, P_{m4} from an upper half portion of the circuit and $P_{m1b,}$ P_{m3b} from lower half portion to operate the circuit, that is they are in ON position two sources connected in series, remaining all are in OFF position. Voltage ($-3V_{S1}$ /2) is applied across the load.

The switching functionality of the proposed single-phase 7-level cascaded hybrid multilevel inverter is realized by thelogical NOT, AND, OR gates, which are as given following pulse generating circuits.

Table 1 Switching sequence

Pm1/Pm1b	Pm2/Pm2b	Pm3/Pm3b	Pm4/Pm4b	Max input voltage
1/0	0/1	1/0	0/1	$3V_{s1}/2$
1/0	0/1	0/1	0/1	V_{s1}
0/1	0/1	1/0	0/1	$V_{s1}/2$
0/1	0/1	0/1	0/1	0/1
1/0	1/0	1/0	1/0	$-V_{s1}/2$
0/1	0/1	0/1	1/0	$-V_{s1}$
0/1	1/0	1/0	1/0	$-3V_{s1}/2$

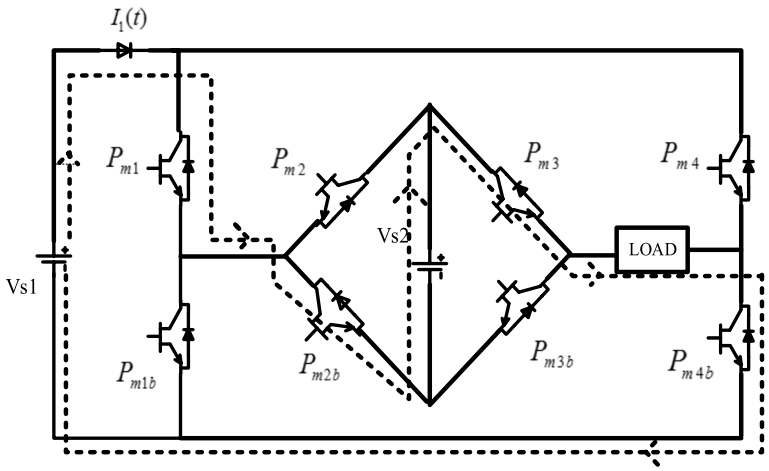

Fig. 2 The output positive voltage at maximum (3VS1/2)

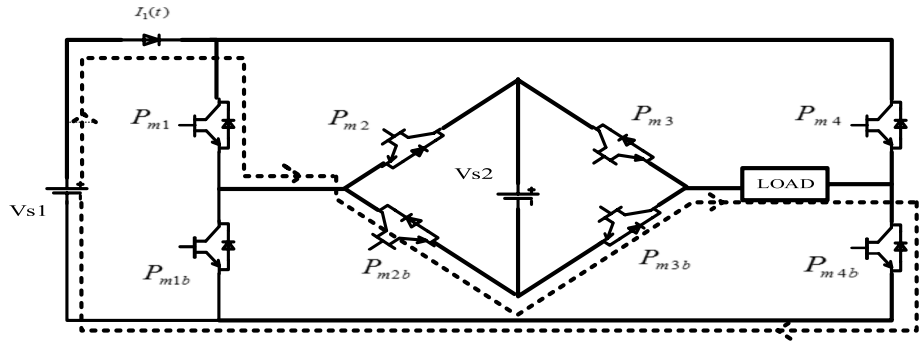

Fig. 3 The output positive maximum voltage of 2/3 of VS1

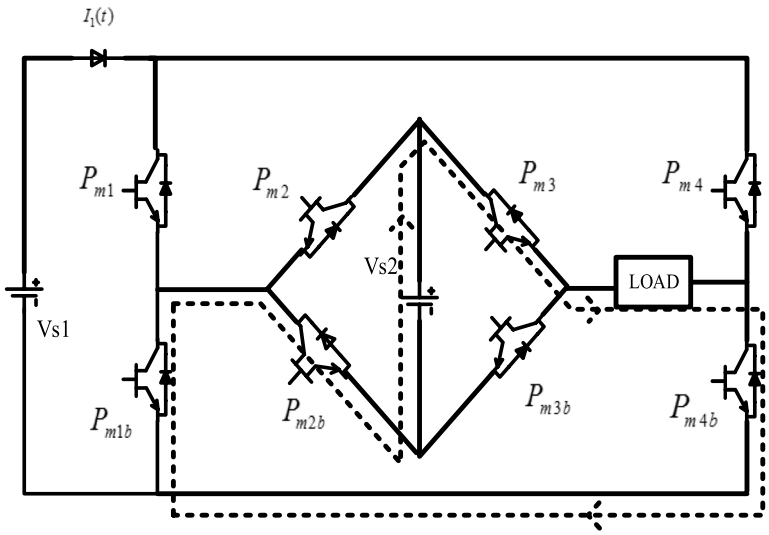

Fig. 4 Output positive maximum voltage of 1/3 of VS1/2

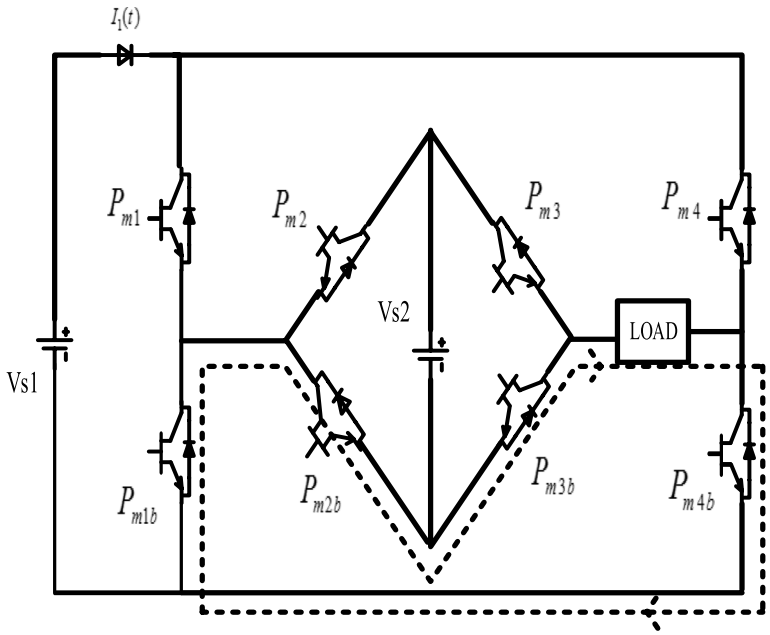

Fig. 5 The output of the circuit is zero

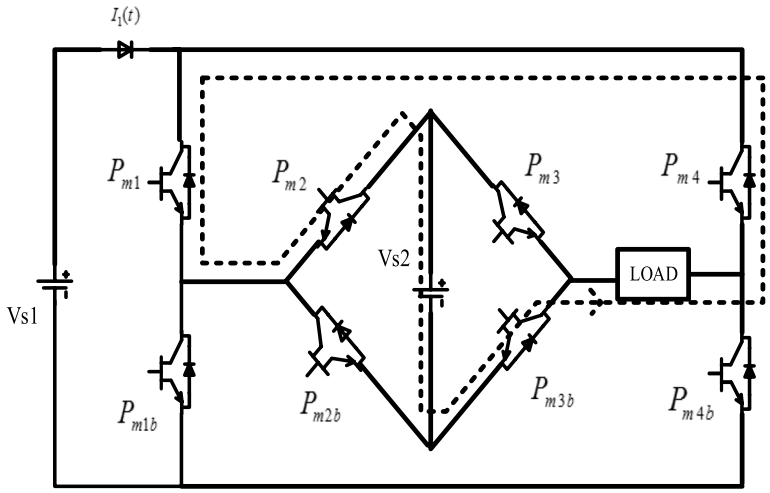

Fig. 6 Output negative maximum voltage of 1/3 of (-VS1/2)

Governing equations

$$P_{m1} = [r_2.c_2 + r_3(c_{14} > ref_1) + \left(Abs(r_1) > c_{12} - \left((Abs(r_4) > c_1).\ (r_1 > \bar{c}_{14})\right) + ((Abs(r_1) > c_{12} - c_{13}).(r_1 < c_5) > c_{14})\right] \quad (1)$$

$$P_{m2} = [(Abs(r_1) > c_{12}) + ((Abs(r_4) > c_1) - c_1).((Abs(r_1) > c_{12}) - ((Abs(r_4) > c_1)).((Abs(r_4) > c_1)) + (r_1 < c_{14}) \quad (2)$$

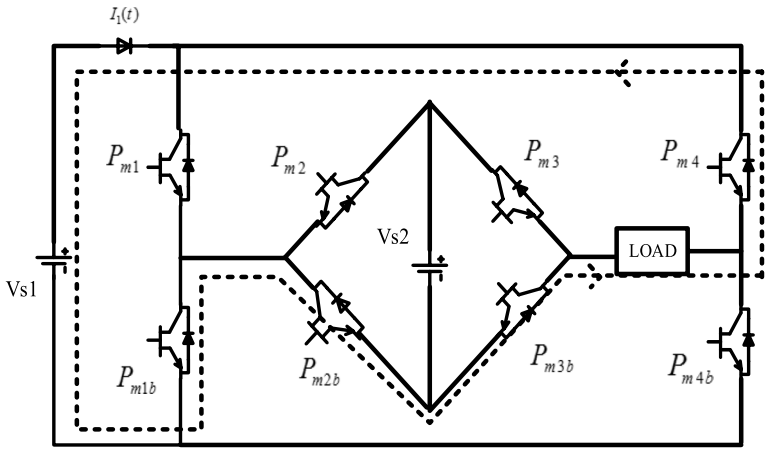

Fig. 7 Negative maximum output voltage of 2/3 of (-V_{S1})

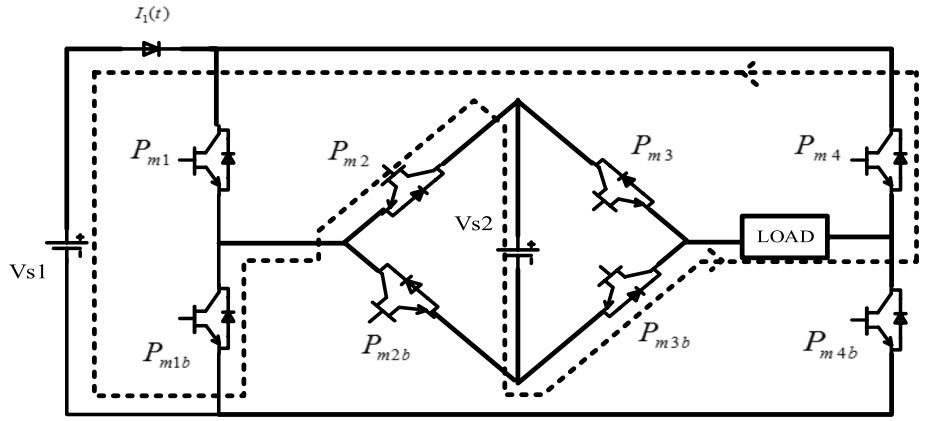

Fig. 8 The negative maximum output voltage of -3VS1/2

$$P_{m3} = \{\left[\left((Abs(r_1) > c_{12}) - (Abs(r_4) > c_1)\right) - c_{12}\right).+\left[(Abs(r_4) > c_1).\left(T_{g1} > Abs(r_5)\right)\right)\right].\left[ref_1 > c_{14}\right)]]\} + \{[((Abs(r_4) > c_1) - c_{13}).(\overline{T_{g1} > Abs(r_1)})] + [Abs(r_1) > c_1).(\overline{T_{g1} > Abs(r_1)})] + [Abs(r_1) > c_{12}) - (Abs(r_4) > c_1)].(r_1 < c_{14})]\} \quad (3)$$

$$P_{m4} = P_{m2} \quad (4)$$

$$P_{m1b} = \overline{P_{m1}} \quad (5)$$

$$P_{m2b} = \overline{P_{m2}} \quad (6)$$

$$P_{m3b} = \overline{P_{m3}} \quad (7)$$

$$P_{m4b} = \overline{P_{m4}} \quad (8)$$

where P_{m1}, P_{m2}, P_{m3}, P_{m1b}, P_{m2b}, P_{m3b} are the gate pulses applied for the control circuit, R is the reference waveform, C_1, C_2, $C_3$is the carrier waveforms of 0,1,2,3,-1,-2,-3 respectively. The following figure shows the reference signals with carrier signals along with pulse waves.

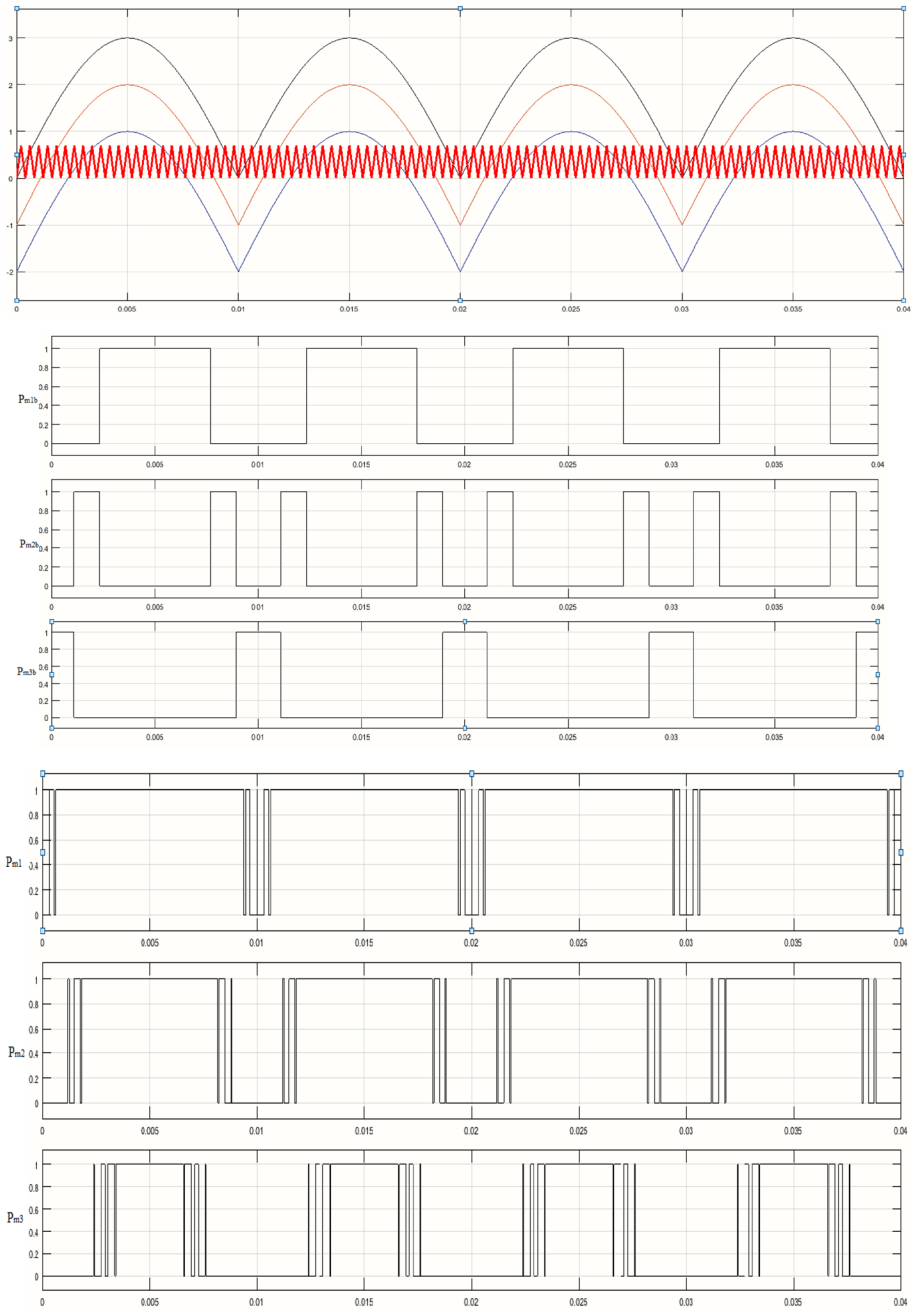

Fig. 9 Reference signals and carrier signal with corresponding gate pulses

Switching scheme (Fig. 9)

Results and discussion

The proposed single phase inverter is simulated in MATLAB r2016a Simulink on a computer with i3 2.3 GHz processor with 4 GB RAM running Windows 8.1 operating system.

Operation of MLI under Depreciating Sources Condition Effect of Fluctuation in Input.

The simulation outputs of the output voltages when the input sources performance deteriorates to fifty percent of its rated design value are shown in Figs. 10, 11, 12 and 13. The resultant harmonic distortion is also being shown and a tabular column comprising the output voltage has been shown along with the graph.

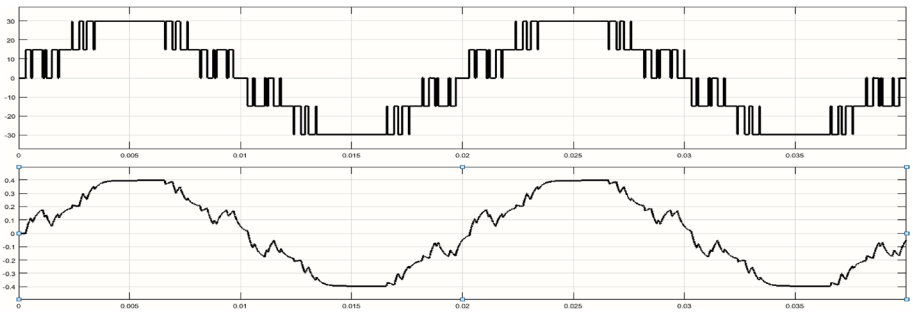

Fig. 10 voltage waveform

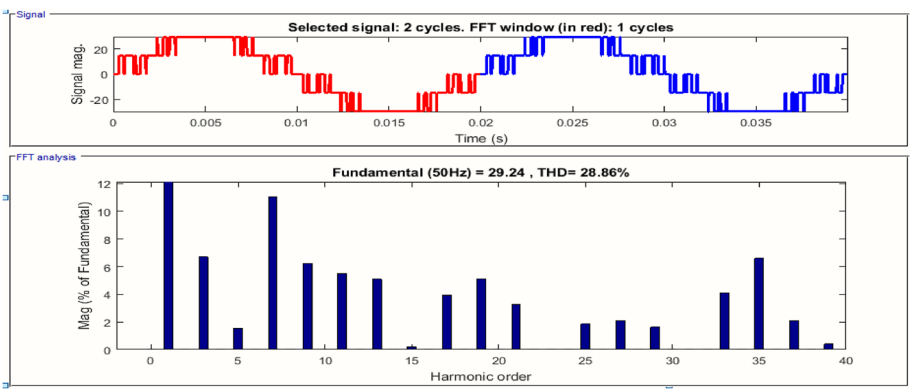

Fig. 11 FFT Analysis of the output voltage waveform, when I[st] Source fall down to 50%: THD = 28.86%

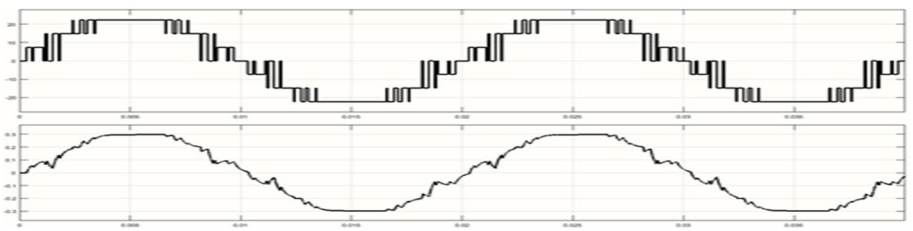

Fig. 12 Voltage waveform

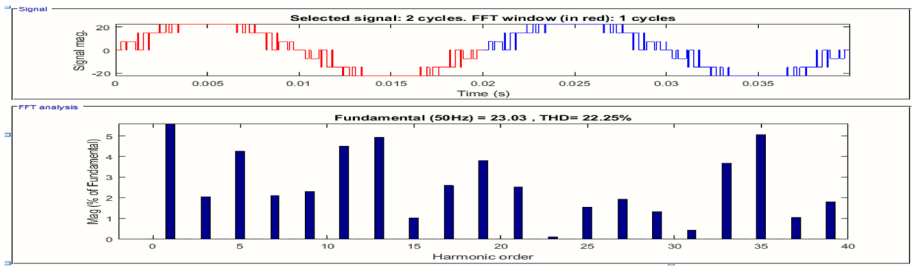

Fig. 13 Harmonic spectrum analyses of the line-line voltage of 22.5 V

Case 1: Ist source fall down to 50%: (15 V, 15 V)

The above Fig. 10 voltage waveform represents when one of the sources sudden drops into half of its original, correspondingly that much voltage drops down and that is shown as 29.70 V, and voltage levels are changed as five levels so that operation undergoes little bit differ from the normal operation. Representative voltage waveform for voltage 29.70 V with 5 levels and peak to peak, RMS Values are observed as 59.39 V and 21.52 V.

From the above figure, we can observe that current is measured as 0.39A which differsfroman original current waveform, from this observation circuit performance depends on working. From the figure, small spikes are observed in the current wave. Current waveform for current 0.39A and peak to peak, RMS Values are observed as 0.79A and 0.27A.

From the above Fig. 11 Harmonic spectrum of the line-line voltage of 28.86%THD. The fundamental frequency and the carrier frequency of 50 Hz and 2 K Hz with a THD of 28.86% are shown in Fig. 11.

The above Fig. 12 voltage waveform represents when input source suddenly drops into 22.27 V of their original, correspondingly that much voltage drops down and that is shown as 22.27 V, but voltage levels are not changed so that operation goes as normal. Representative voltage waveform for voltage 22.27 V with 7 levels and peak to peak, RMS Values are observed as 44.54 V and 16.68 V. From the above Fig. 12 we can observe that current measured as 0.29A, the waveform shows a little bit distortion from original current waveform, from this observation negligible count of distortion is there so that system does not undergoes any deformation in its operation, and Figure Represents current of 0.29A and peak to peak current value is 0.59A, RMS Value is observed as 0.21A. Representative voltage waveform for voltage 22.27 V with 7 level and peak to peak, RMS Values are observed as 44.54 V and 16.68 V and current waveform for current 0.29A and peak to peak, RMS Values are observed as 0.59A and 0.21A.

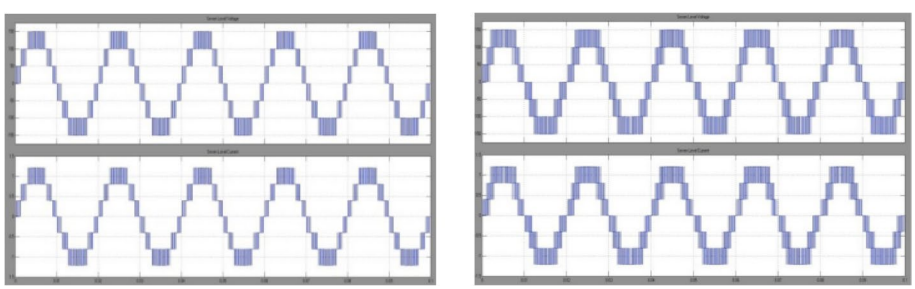

Fig. 14 Output with R and RL load

Table 2 Voltage THD (%) of hybrid multilevel inverter for R load

	7-Level				9-Level				11-Level			
	Without Filter		With Filter		Without Filter		With Filter		Without Filter		With Filter	
Ma	APOD	CO	APOD	CO	APOD	CO	APOD	CO	APOD	CO	APOD	CO
0.85	12.21	14.71	1.10	6.97	8.96	11.54	0.78	6.25	7.34	9.93	0.72	5.59
0.9	11.56	13.88	1.02	6.38	8.53	10.84	0.83	5.71	7.00	9.15	0.71	5.01
0.95	11.12	12.99	0.99	6.04	8.37	10.25	0.74	5.37	6.52	8.51	0.71	4.71
1	9.70	12.08	0.86	5.83	7.44	9.47	0.69	5.22	6.02	7.79	0.66	4.65

Case 2: second source fall down to 50%: (15 V, 7.5 V)

From the Fig. 12, we can observe that current measured as 0.29A, the waveform shows a little bit distortion from original current waveform, from this observation negligible count of distortion is there so that system does not undergoes any deformation in its operation, and Figure Represents current of 0.29A and peak to peak current value is 0.59A, RMS Value is observed as 0.21A. Representative voltage waveform for voltage 22.27 V with 7 level and peak to peak, RMS Values are observed as 44.54 V and 16.68 V and current waveform for current 0.29A and peak to peak, RMS Values are observed as 0.59A and 0.21A.

Figure 13 Harmonic spectrum analyses of the line-line voltage with fundamental frequency and carrier frequency of 50 Hz and 2 kHz with a THD 22.25% are shown in Figure. When voltage source 1's input is at a loss of 50%, i.e. the voltage output of the designed source is diminished to half of its rated value, the output parameters have changed, the THD is 22.25% and the number of voltage levels is 7. The observations noted that overall loss of 50%. of the THD is almost equal to rated output voltage; it is observed in cascaded multilevel inverters. The Fig. 14, represents the output with R and RL load with seven levels and Table 2 determine the voltage THD (%) of hybrid multilevel inverter for R load. The total output voltage of the HMLI inverter, shown in Fig. 15, is the sum of the vab and vbo of the H-bridge and CCM, respectively.

Conclusions

The proposed MLI significant role in minimizing the number of higher frequency switching devices. The system operated at a sudden drop in voltage half of its rated voltage, the changes in the system behavior observed, the voltage, current, and corresponding THDs are noted. The results noted that an overall loss of 50% of the THD is almost equal to rated output voltage, it is observed mostly in cascaded multilevel inverters. A new topology of seven-level cascaded MLI was proposed with excellent characteristics over conventional multilevel inverters with the reduced part count, separate dc sources, and reliability. This newly proposed topology is structured with eight switching devices from those four switching for the production of seven voltage levels. This topology has more applications in the power sector as well as industrial applications such as HVDC and solar photovoltaic systems. This topology easily collaborates with grid and equal load sharing, the number of switches operated simultaneously to collectively produce different voltage levels. Four of the eight switches operated at a fundamental frequency by minimizing the

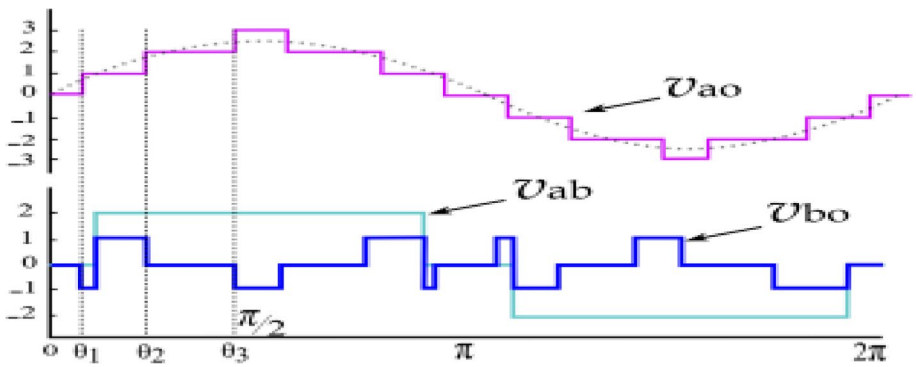

Fig. 15 Sum of the vab and vbo

switching losses. The use of isolated dc sources accessing renewable energy applications. The implemented seven-level model specifies its applications in medium voltage inverters for driving the motor, PV cells working at high frequencies. The simulation results in MATLAB have verified the analyzed for the asymmetrical multilevel inverter.

Abbreviations

SPWM	Sinusoidal Pulse Width Modulation
THD	Total Harmonic Distortion
MLI	Multi Level Inverter
RMS	Root Mean Square
HVDC	High-Voltage Direct Current

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Authors' contributions
BP and SK – Conceptualization, Methodology, Visualization, Analysis, Writing- Original draft preparation. Data correction, Investigation on various cases and Validation of results. PRK and ARS– Resources, Writing—Review & Editing the article and validation of outputs. All authors read and approved the final manuscript.

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Declarations

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